Presentation by KC0JFQ

KC0JFQ presents:

ICARC FOX Transmitter 102-73181-10 Latest (probably the last) Fox Transmitter Design

H t t p : //www.icarc.org/icarc\_foxhunt.htm H t t p : //n952.ooguy.com/HamRDF/index.html H t t p : //n952.ooguy.com/eagle/index.html

Presentation by KC0JFQ

## WORK BACKWARDS!

## RF amp ← Frequency Synthesizer ← Control

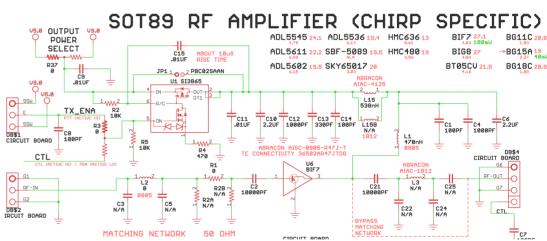
http://n952.ooguy.com/eagle

Presentation by KC0JFQ

### **RF** Amplifier Selection

Power level Bandwidth Implementation

http://n952.ooguy.com/eagle

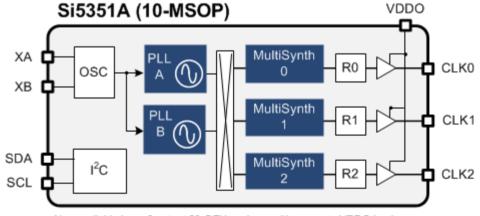


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## **Frequency Synthesizer Selection**

Component life Support Tools Bandwidth

http://n952.ooguy.com/eagl



Also available in an 8 output 20-QFN package with separate VDDO banks

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**Control System Selection** 

## Raspberry Pi ARM SOC processor (ZiLOG ZNEO) PIC processor (low cost)

http://n952.ooguy.com/eagle

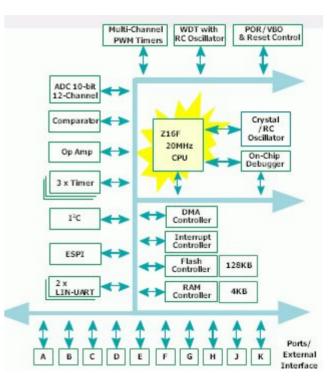


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Control System ZiLOG ZNEO

Hardware FRAM/FLASH memory TOY Clock

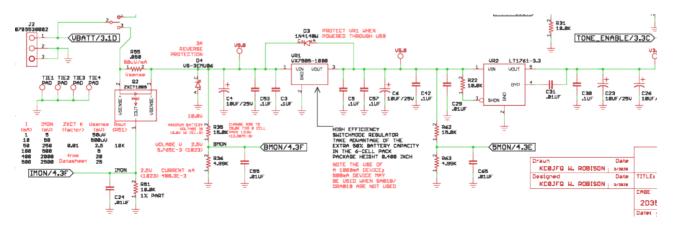
http://n952.ooguy.com/eagle



Presentation by KC0JFQ Control System ZiLOG ZNEO

Hardware Power Conditioning Power Monitor

http://n952.ooguy.com/eagle

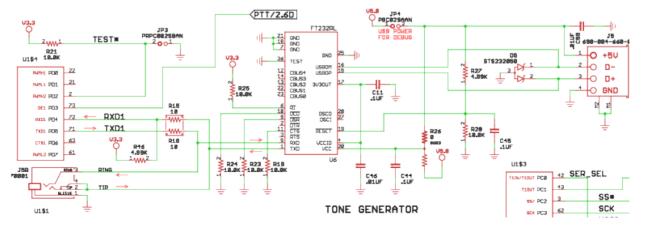


Presentation by KC0JFQ

Control System ZiLOG ZNEO

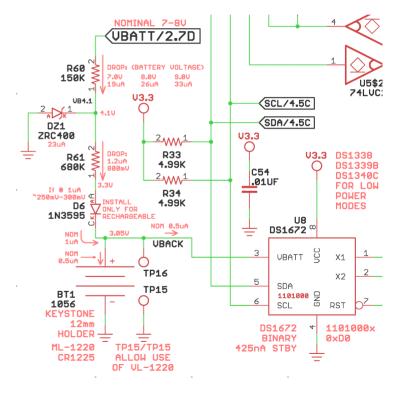
#### Hardware Local Communications

### http://n952.ooguy.com/eagle



Presentation by KC0JFQ

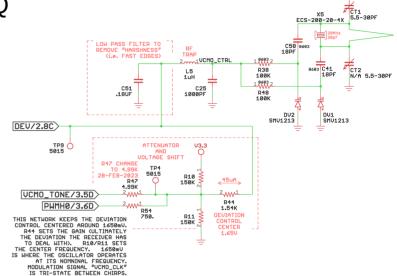
Control System ZiLOG ZNEO Hardware TOY Clock http://n952.ooguy.com/eagle

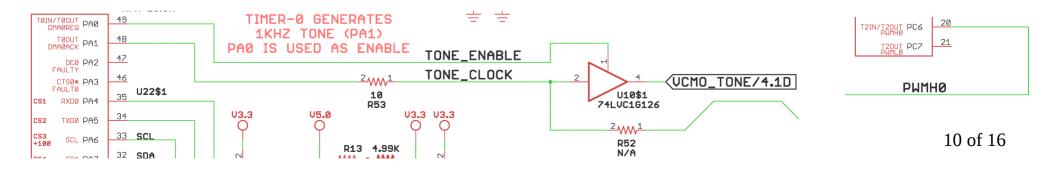


#### Presentation by KC0JFQ

### Control System ZiLOG ZNEO

Hardware Modulation/Deviation Control http://n952.ooguy.com/eagle

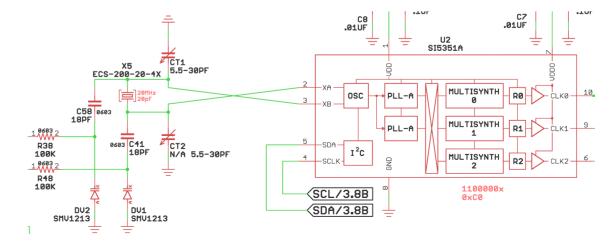


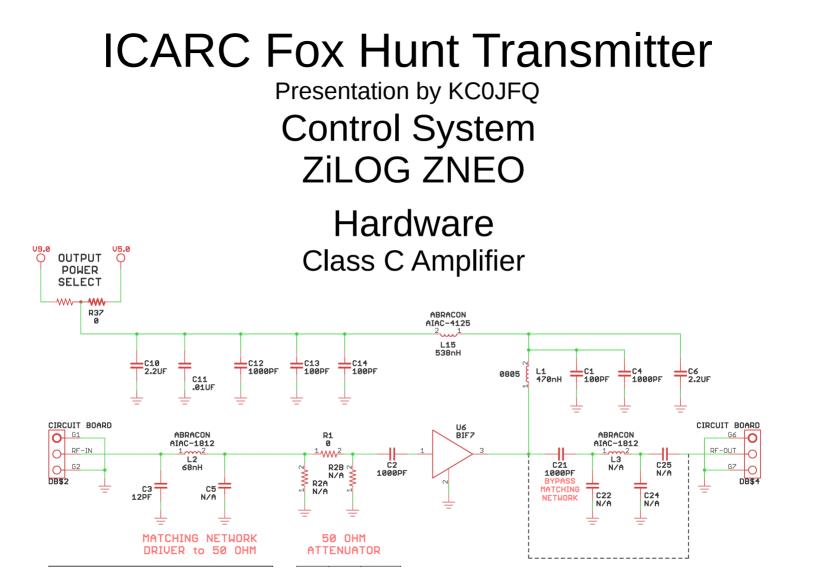


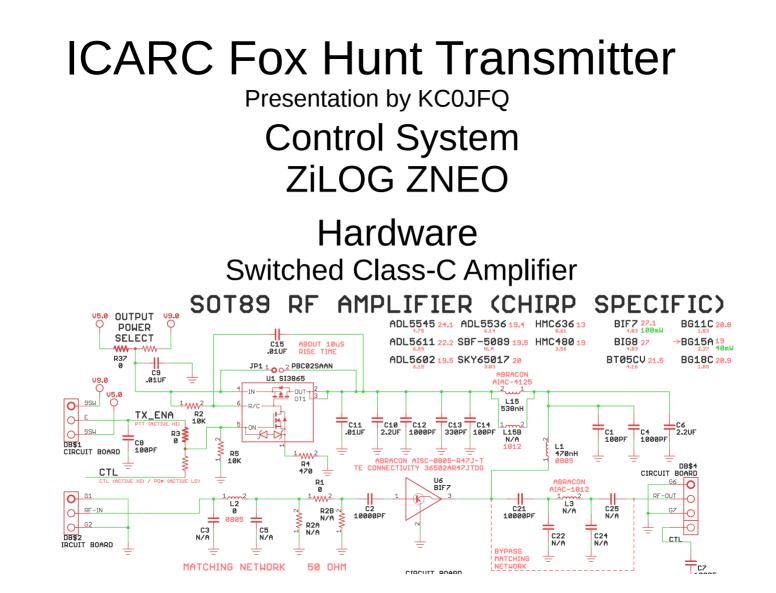
#### Presentation by KC0JFQ

### Control System ZiLOG ZNEO

#### Hardware Reference Clock http://n952.ooguy.com/eagle



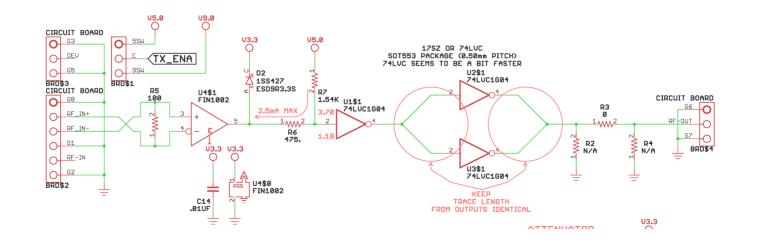




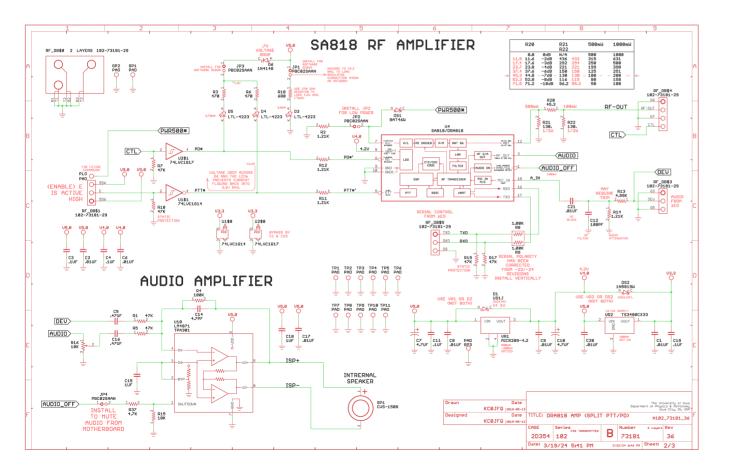
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Control System ZiLOG ZNEO

Hardware Class D Amplifier



#### Presentation by KC0JFQ



### Control System ZiLOG ZNEO Hardware RF tranceiver module

Presentation by KC0JFQ

Control System ZiLOG ZNEO

Hardware No Amplifier at all



Presentation by KC0JFQ

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Here we go again!

Discussion of ICARC FOX Transmitter by KC0JFQ

This is the culmination of a series of transmitters, with the goal of being easily configured for any style of fox hunting event.

ICARC currently has 12 of the latest revision transmitters.

Latest hardware and software development essentially complete. Incorporates all the features of the previous models. Adds more operating modes.

Successful hunt conducted with the new hardware 4/2024.

TWELVE 102-73181-10 units!

Presentation by KC0JFQ

#### WORK BACKWARDS!

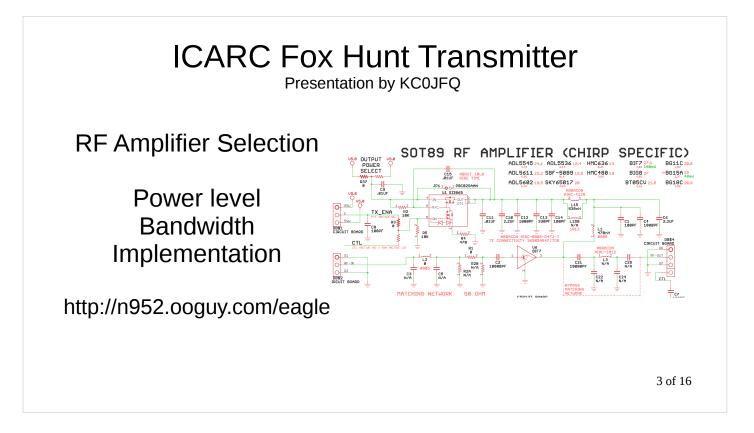
#### RF amp ← Frequency Synthesizer ← Control

http://n952.ooguy.com/eagle

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We'll work backwards as I think that will make life easier.

These are battery powered (of course) so battery life can be an issue. Has to last through the entire event. Don't want to be buying batteries for each event. Will talk about battery selection towards the end.



What power level do we want?

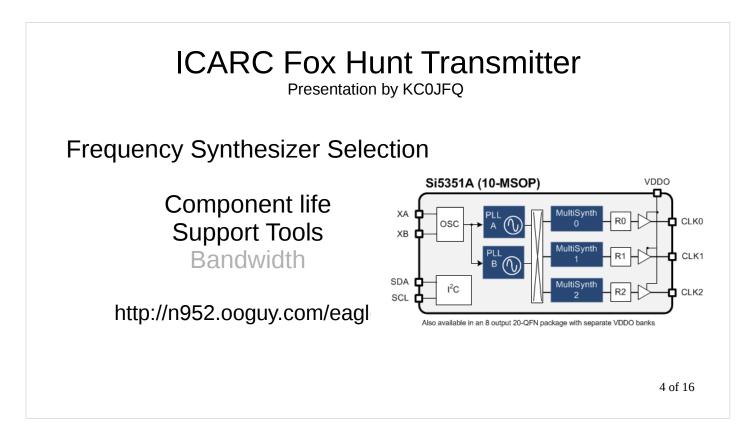
10mW to 50mW works in a small area (Hickory Hill Park). 100MW to 500mW in large area (Kent Park).

5mW or so can be obtained directly from the synthesizer output pin. 10mW to 50mW can be obtained from paralleled high speed CMOS logic gates (74LVC04).

50mW to 100mW using an MMIC (monolithic microwave integrated circuit), essentially a really fast RF transistor matched to 50 ohms.

100mW to 1000mW from the RF transceiver module.

All require low pass filter to suppress harmonics (LPF is on the mothterboard).



Pick one and it will likely be obsolete next year :-(

ICS525 and ICS307 were used in early units, none are available any longer (they kinda sucked anyway...).

Switch to SI5351 in the 102-73181-5 <sup>(C)</sup>. It is in production and far more flexible (i.e. programmable) than the ICS525/ICS307. Can hit all the 2M frequencies. Frequency calculation a bit involved, but the register values are pre-calculated with the resulting values saved in program flash in the Fox Transmitter System.

A frequency counter is useful when generating register patterns for the SI5351! (i.e. check your work and).

SA818/DRA818 is a low-cost (<\$15.00) RF transceiver module. Output 500mW or 1000mW. We program this with very simple ASCII text string. (most seem to be way less than 500mW).

A utility was produced to calculate the register values for the SI5351 multi-synth. Small table in zNEO flash, we can load anything through the serial port (or from FRAM).

Presentation by KC0JFQ

#### **Control System Selection**

Raspberry Pi ARM SOC processor (ZiLOG ZNEO) PIC processor (low cost)

http://n952.ooguy.com/eagle



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Large universe of SOC devices to choose from.

The ZiLOG ZNEO is what I settled on. This device Implements a Harvard bus architecture with a VonNeumann address space. Split instruction and data (i.e. seperate FLASH and RAM datapath) for access concurrency, with an instruction set that doesn't access these two spaces with different instructions (compiler-friendly).

The ZNEO selection is an outgrowth of the RIME/REASON GSE that started out life using a ZiLOG eZ8 processor (pure Harvard architecture). Software was getting too complex when dealing with Harvard-isms. This forced a change to ZNEO mid-stream (chip pinouts on the eZ8 matched the ZNEO saving circuit board rework).

All the 73161/73181 Fox Transmitter systems use the ZNEO.

The 102-73181-10 revision changes zNEO packages (now a 64 pin LCC) due to availability.

#### **ICARC** Fox Hunt Transmitter Presentation by KC0JFO Multi-Channel WDT with BC Oscillate POR/VBO & Reset Cont Control System ADC 10-bit L2-Channel **ZILOG ZNEO** 716F Op Amp Hardware FRAM/FLASH memory TOY Clock 128KB http://n952.ooguy.com/eagle 6 of 16

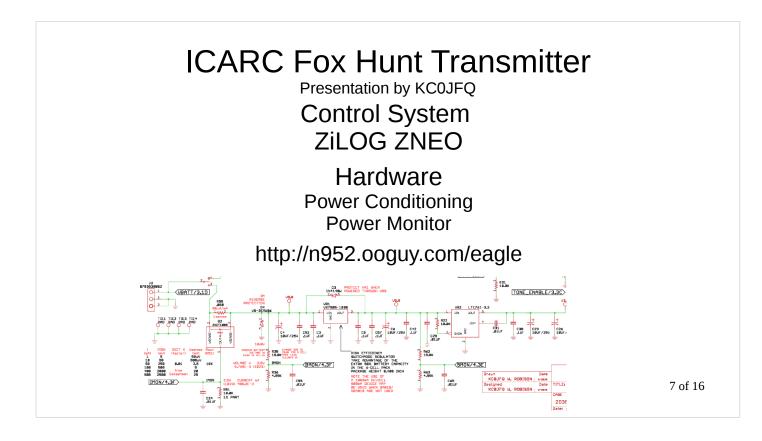
The ZNEO has 128KB of program flash and 4KB of data RAM (currently the control program is over 100K!).

ZiLOG provides development tools: c-compiler and linker and a low-cost programming device (ethernet connection to host). The build environment is hosted on a Linux box (using WINE).

External to the ZNEO are two *serial* memory devices, one FRAM and one FLASH. The operating schedule (commands) is in FRAM (easy/fast to change, but \$\$.\$\$) and the audio clips are in FLASH (large device for less than \$1.00).

These two device live on the zNEO SPI bus. The ZNEO provides the bus controller that is used to access these two devices.

Clock chip uses a 32,768Hz oscillator and a 15+32 bit counter. 15 bit counter divides the 32KHz to 1HZ and the 32 bit counter counts seconds from some epoch. Backup battery (coin cell) is charged by the main battery at a ve**rrrrr**y low rate (less than 1uA). Main battery keeps backup cell from discharging. Clock allows *set & forget* Foxhunt setup!



The system is powered by a six to twelve cell battery pack. Nominally a 6-cell AAA pack fits in the housing. A rechargeable pack could also be used.

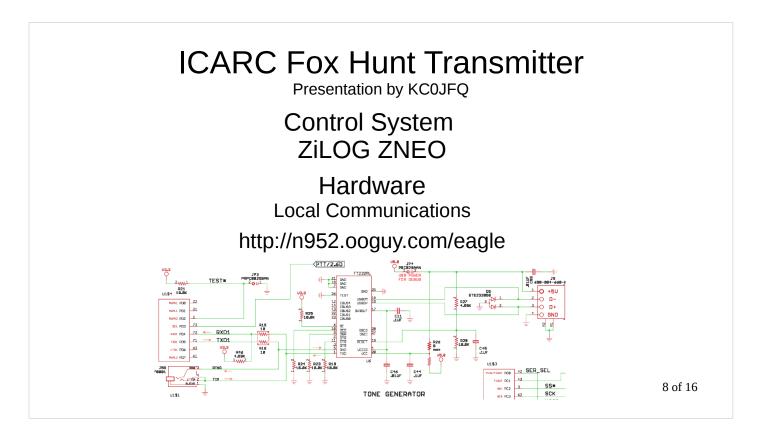
A switch mode converter is used to produce the main 5V rail to minimize heat and wasted battery power (efficiency north of 90%). Device VR1 must be selected to supply adequate power to the RF daughterboard (DRA818 is a power pig).

A current sense circuit (Q2/R55) measures current from the battery, and voltage (R35/R36) at the battery. There is an additional voltage sense on the 5V rail (R62/R63).

3.3V for the ZNEO is provided by a low-cost low-dropout **linear** regulator (VR2). ZNEO is the primary load on the 3.3V rail. Logic gates on the motherboard are also powered by the 3.3V rail.

The RF daughterboard receives the regulated 5V rail and the raw battery voltage (both are switched). RF section is powered only during transmit.

The SA818/DRA818 take forever to wake up following application of power.

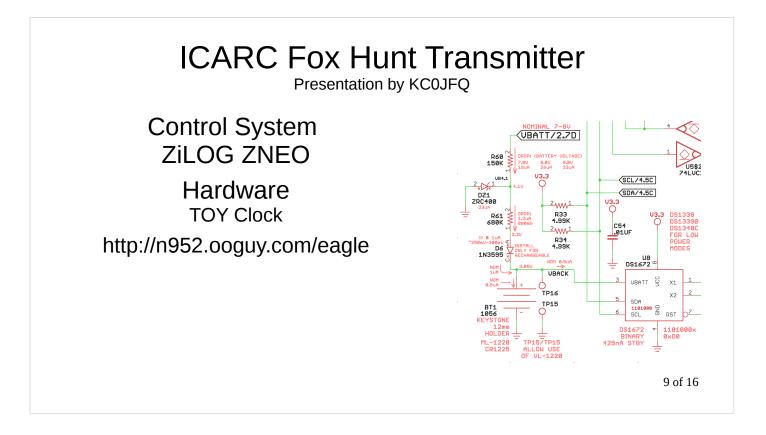


Connection to a host system (for FRAM/FLASH programming) is provided using one of the ZNEO serial ports (UART1).

This control port may be implemented as a USB serial port (J5) or a simple buffered Tx/Rx pair (J4). USB uses the FTDI FT232RL device. Use a USB to serial converter cable to connect to the buffered port (lower cost, easier to use).

A second serial port is buffered and routed to the daughterboard. This second serial port is dedicated to controlling the daughterboard (i.e. the SA818/DRA818 or an external tranceiver).

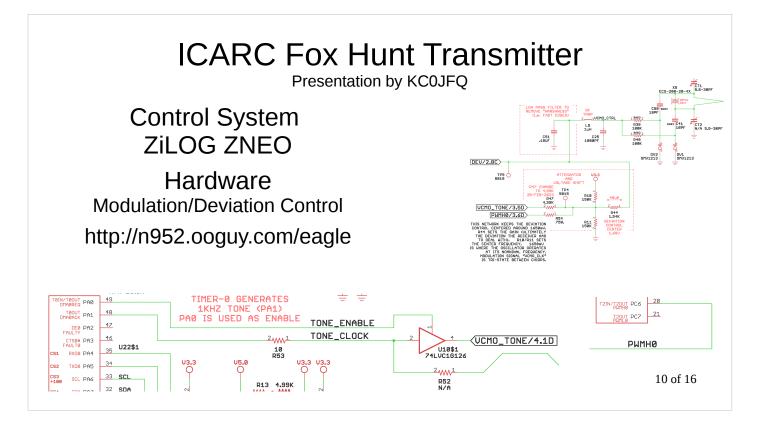
There was a network time function that appeared on previous models, it has been deprecated (never used it in the field). UARTO talks to SA818/DRA818. The 3.5mm port on motherboard (that was the network time function previously) now accesses UART1. Setup is much faster when you don't have to open the case! FTDI cable: TTL-232R-3V3-AJ



Time synchronization makes use of a TOY (time of year) clock. U8 is a 32 bit counter that ticks at a 1 second rate. Software reads clock at startup, copying it to the system time and then maintains the system time (also a 32 bit integer).

The string of parts on the left keep the backup battery charged from the main battery. R60/DZ1 form a crude 4V regulator. Using the 4V net, R61 limits charge current and D6 isolates the backup battery from the main battery. Should be less than 1uA or charge current to the backup battery.

Operating schedules rely on the time from the TOY clock. So the TOY would normally be set the night before. Uncorrected drift is limited to a few seconds per day. All the TOY clocks are synchronized, so no additional synchronization is required at the fox hunt! Turn on the transmitter, listen for the **alive** message, and you're free to move on to the dropping the next station.

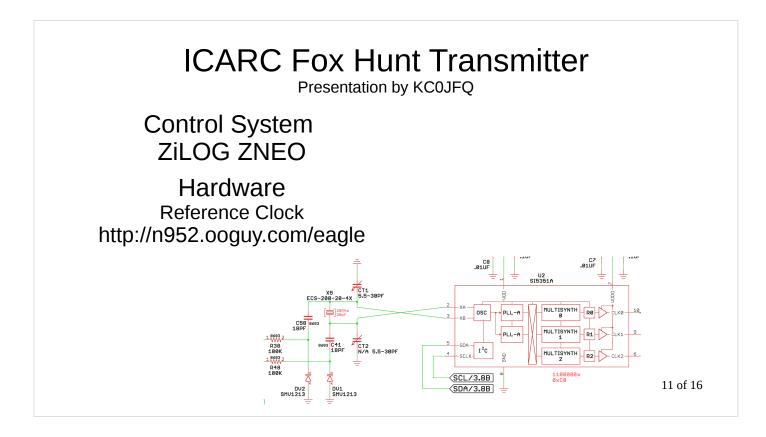


The ZNEO provides for two methods of supplying audio to the RF deviation control.

One is a simple square wave from a programmable clock/timer source in the ZNEO. This tone is gated through a buffer (U10) to allow for simple on-off control using a single port bit (this is the CW audio tone generator). The **TONE\_ENABLE** signal is also used in other parts of the circuit, so it's not quite overkill.

A PWM controller (lower right corner) in the ZNEO may also be used to control the transmitter deviation.

The data stream to control the PWM channel is stored in the FLASH device. Byte samples are read from the FLASH and written to the upper 8 bits of the PWM register. Sample rate is controlled by setting the SPI clock rate. Latest software deals with rates of 4K, 5K, 8K, 10K, and 16K samples/second (we normally use a sample rate of 4KHz in the ICARC transmitters).



The reference clock for the SI5351 come from a lowcost crystal (20MHz to match the zNEO crystal). The load capacitors on the crystal are varactor diodes (i.e. voltage controlled capacitors or PIN diodes). The deviation control signal reverse biases the diodes which affects the junction capacitance thereby pushing and pulling the crystal frequency.

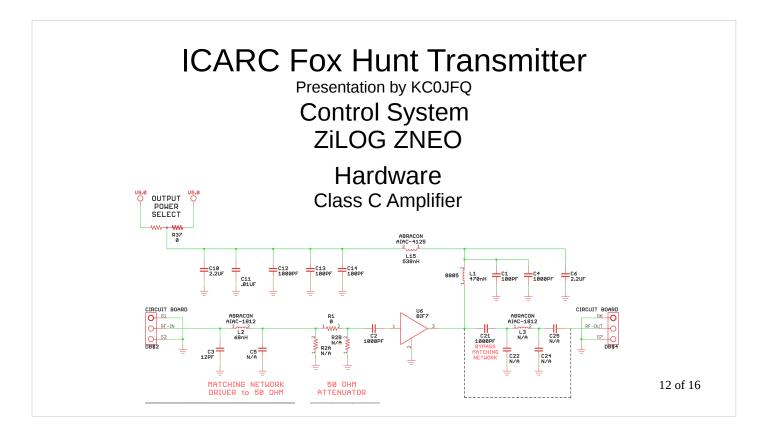
The SI5351 PLL chases the (varying) reference clock (X5) producing the FM modulation of the carrier. The output of the SI5351 is fed to the daughterboard for further amplification.

One channel is raw from the SI5351.

The second channel is buffered and level shifted to 5V.

These first two channels share a connection to the RF daughterboard.

The third is buffered through an LVDS driver.



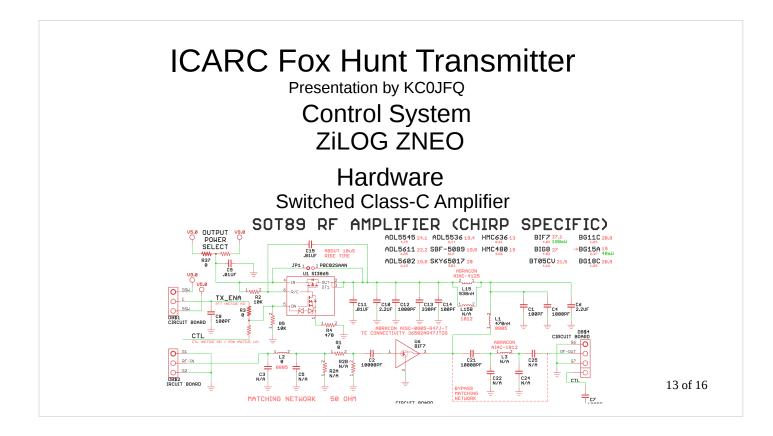
The RF daughterboard sits above the output filter on the motherboard.

One connector (DB\$1 is not shown) provides switched power, both the regulated 5V rail and the unregulated battery voltage.

The RF comes from the motherboard (DB\$2) and is routed to the gain block through an impedance matching network (C3, C5, L2), and attenuation network (R1, R2A, R2B), and a blocking capacitor (C2).

The output of the gain block is passed through another impedance matching network (C22, C24, L3) and the back to the low pass filter on the motherboard. The antenna connector (BNC) on the motherboard sits after the LPF.

This amplifier is capable of producing over 100mW when connected to the SI5351.



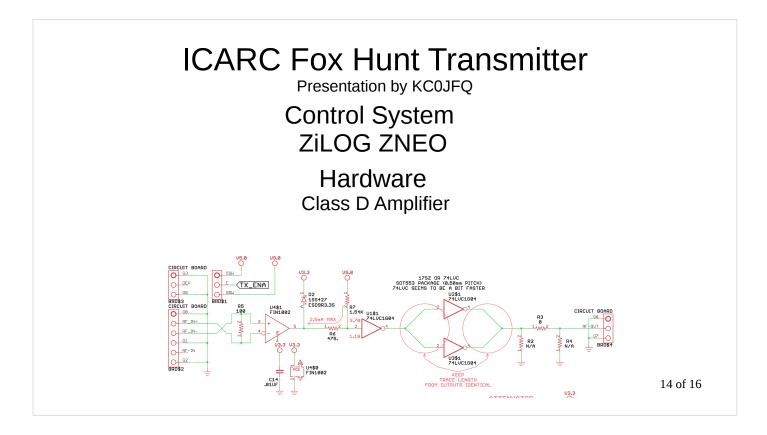
This RF amplifier, almost identical to 103-73161-28, is used to emulate a wildlife tracker and to operate A1A. The power to the RF gain block is switched by U1. The tracker mode is enabled using the **CHRP** command which causes the PTT\*/TX\_ENA signal to be asserted only when a chirp is being sent. Quiet time between chirps does not send RF.

The transmitter may operate in A1A mode using the **CONF CW** command and disabling audio modulation using the **FREQ 0.0** command.

The power switch (U1) is setup to *soft start* to limit the transient load presented to the 5V regulator on the motherboard and to soften the RF switching.

Like the other Class-C amplifiers, there are matching networks on input and ouput as well as an input attenuation network. The list of gain blocks (all are MMICs) are all 50 ohm input and output. The SI5351 output can be configured as a 50 ohm source.

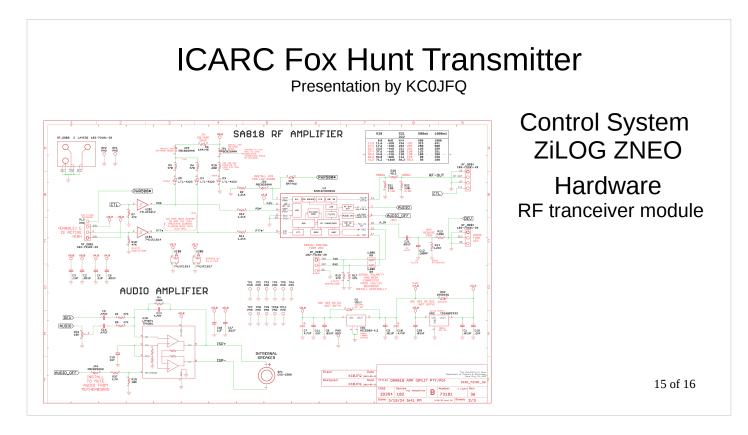
This amplifier produces from 40mW(BG15A) to over 100mW(BIF7) when connected to the SI5351.



This RF daughterboard uses the LVDS channel that is provided on the 102-73181-10 motherboard.

It is a simple class-D amplifier that uses a high speed CMOS buffer as an amplifier. The 74LVC gates are all powered from the 5V rail (to slightly increase power). There is a level shifting network between the LVDS receiver and the first 74LVC gate (R6, R7).

The 74LVC1G04 gate is carefully chosen for very low propagation delay (try a Diodes Incorporated 74LVC1G04W5-7) as we operate the gate at 150MHz, at the very edge of its performance envelope. Signals out of the 74LVC1G04 exhibit poor rise times, but this reduces higher order harmonics, which is to our advantage.



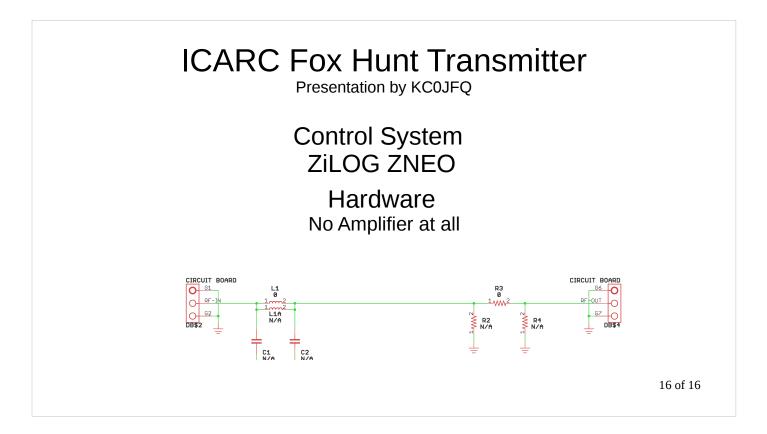
The SA818/DRA818 walkie-talkie module is an almost complete radio subsystem. Implementing both transmit and receive, we use only the transmit function. This module requires only a low-pass filter on its antenna pin (provided on the motherboard) to be fully functional.

We remove power from the daughterboard between message transmission to reduce power. The module takes about 1000 to 1500 mSec to *wake-up* when powered.

System power draw is typically just above 300mA from the battery during transmit.

The SA818/DRA818 can be programmed for almost any frequency.

At the 100mW power level, the MMIC amplifiers offer considerably lower operating power.



The synthesizer output may be run *naked*, right out to the antenna through the low pass filter on the motherboard using this board.

The board has an impedance matching section and an attenuator section, either of which may be bypassed.

The board also has a 5V monitor LED that can be useful in debugging hardware issues and for software development.

Due to the way RF is managed, the *wildlife tracker* and *A1A* operation is not possible with this daughterboard.