ICARC Fox DTOA Receiver

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This is the start of a manual for the ICARC *FOX DTOA Receiver*.

It is a work-in-progress right now so suggestion for updates may be sent to **kc0jfq@n952.ooguy.com**.

Full size documents may be found here: http://n952.ooguy.com/eagle

http://n952.ooguy.com//home/wtr/eagle/JUICE/A102_73161/FOX_ICARC.tex

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1 Glossary of Terms

There is an attempt being made to use some terms in this document in a precise manner. Some of the discussions become a bit muddled when terms are used casually.

1.1 FRAM

Ferro Magnetic **R**andomn **A**ccess **M**emory.

A type of non-volatile memory that exhibits symmetric access speed. IN other words the write speed is the same as the read speed.

1.2 zNEO Processor

This refers to the zNEO system-on-chip. It has an instruction execution engine (i.e. the CPU), program memory, data memory, and a variety of peripherals.

1.3 Sequence

We will use the term **SEQUENCE** in this document to a set of instructions that executed as a group.

Typically this *sequence* is stored in external memory.

1.4 TOY Clock

Time-of-Year clock. A battery backed clock that keeps time when the *FOX DTOA Receiver* is not powered.

1.5 xxx

xxx

2 Motivation

Why do we do it?

Because we can!

Looking for an inexpensive direction finding radio that doesn't require an expensive handheld for operation. We have rolled a commodity VHF receiver and a DTOA antenna switch into one unit.

2.1 Requirements

These are required for operation.

2.1.1 Operates in the 2M Band

FM Receiver.

DTOA Switch.

Internal Speaker (self contained operation).

2.1.2 Battery Operation

Same as the fox transmitters, operation for several hours using 9V battery or a 6-cell AAA pack.

2.1.3 Code Storage

We must store enough bits to control the receiver.

2.2 Desirements

These are desired features

2.2.1 Voice

We use the PWM controller in the last FOX Transmitter design. Why not make use of this so the receiver can announce configuration changes.

2.2.2 Multiple frequency

We would like to be able to operate the receiver on more than one frequency.

70cm operation.
The DRA818 may be purchased in either 144MHz of 440MHz versions.

3 Theory of Operation

xxx

3.1 Receiver

We use a commercial RF transceiver, either an SA818 or DRA818. This RF module is controlled using a simple serial protocol.

Note that the RF module is a transceiver that is capable of transmitting. Although there is no provision for a microphone, the zNEO drives all the control pins on the SA818/DRA818 RF module. The unit is, therefore, capable of transmitting. The DTOA switch is marginally capable of handling the 500mW output power of the RF module. Transmit power should be directed to J2 to limit spurious emissions.

3.2 Antenna Switch

The antenna switch makes use of a PIN diode to switch between two antenna inputs. Several common cathode devices are available in the SOT23-3 package should the one indicated on the schematic is not adequate to handle transmitting.

3.3 Processor

Having too much memory is a problem that is easily overcome...
Too little memory on the other hand...

ZiLOG zNEO with 128KB program memory (flash) and 4KB data memory(SRAM). USB and Ethernet programmers connect to a 6-pin header to re-flash the zNEO. No software in the zNEO is required to re-flash the processor.

3.3.1 TOY Clock

DS1672.

3.3.2 External Memory

Ferroelectric Random Access Memory. The is the 21st. century answer to core memory. It is non-volatile, like antique core memory, and uses a destructive read cycle. The device operates at wire speed, so it appears a non-volatile random access memory to the zNEO.

A read operation, much like the core memory of decades ago, occurs in two cycles. In the first cycle zeros are written to the memory cell, looking for changes that occur during this cycle, then the data that was just read is written back. A write operation is simply the last cycle of a read.

This foolishness is, of course, fast and transparent. The zNEO simply sends a read command to the FRAM and reads as much data as needed. The write is much the same, an 8 bit command and a 24bit address are followed by as much data as needs to be written. The FRAM then performs the read or write operation and returns any needed data.

3.3.3 DAC

The zNEO has a PWM controller that is used as a limited bandwidth audio DAC. The zNEO controls the sampling rate of this DAC by programming the SPI clock to eight times the sample rate and then moving audio data directly from the FRAM into the PWM duty cycle control register.

3.3.4 UART

The zNEO has two dedicated UART blocks that provide basic serial communications without having to use the processor to serialize data and control timing.

The UART channel to the DRA818 (U1) has current limiting resistors in the two data lines. These allow a misunderstanding about the direction of the data lines to be corrected as well as providing the aforementioned current limit function. The two resistors mounting pads are symmetrical about both the X and Y axis allowing the resistors to be rotated 90 degrees on the pads to swap the TxD and RxD lines.

3.3.5 Timers

The zNEO has three timer channels. Two of these channels are used to support the LCD module. One is configured to generate a voltage to control the LCD contrast. The second is configured as a current regulator for the LCD back-light.

The third timer channel provides the so-called *real time interrupt* that keeps the system time and provides basic interval timing.

3.3.6 I2C

The zNEO has an I2C controller to provide access to the TOY clock.

The TOY clock is only accessed at startup and when time set commands are manually issued, so the zNEO I2C block is not currently used. Rather, the I2C protocol is bit-banged in software.

3.3.7 SPI

The zNEO has an SPI controller.

The SPI control block is used to access both the FRAM and the LCD display.

The FRAM is a non-volatile memory device. A very simple file system is used to store commands and audio data in the FRAM. When accessing commands in the FRAM, the SPI CLOCK is programmed to around a 1MHz to speed access. When accessing audio data in the FRAM, the SPI CLOCK is programmed to operate at eight times the sample rate, normally 64KHz. This limits the data rate from the FRAM to the audio sample rate.

The LCD is also access through the SPI block. It employs a separate *CHIP SELECT* to allow the clock and data pins to be shared with the FRAM.

3.3.8 Edge Interrupts

The zNEO can use up to 8 input bits to trigger an interrupt on an edge change. The 8 bits can be connected to corresponding bits on either port-A or port-D. Three of these bits are used to manage the rotary encoder, one for the button function, and two for the quadrature encoder.

3.4 Controls

controls.

3.4.1 Rotary Encoder

Frequency and configuration selection is accomplished using a simple rotary encoder. The encoder produces a digital quadrature waveform with the signal edges triggering interrupts to track the rotating position of the control.

The encodes also has a switch feature that produces a contact closure by pressing the shaft. This closure also triggers an interrupt.

3.4.2 Volume Control

The volume control is a simple potentiometer at the input to the audio amplifier. It jointly controls the received audio and the internal audio.

3.4.3 Power Switch

This is a simply on-off switch.

3.4.4 Display

2 line 8 character LCD.

xxx.

3.5 External Connections

xxx.

3.5.1 Antenna

BNC.

3.5.2 Audio

3.5mm jack.
Plugging a headset into this jack will mute the internal speaker.

3.5.3 Programming

3.5mm stereo jack.

This is a pseudo-CI-V port. It presents a standard serial interface with logic levels. Polarity matches RS232 but voltage levels are 3.3V and 0V.

3.6 Signal Paths

Description of the signaling paths in the design.

3.6.1 zNEO Reset

U7, a 3 input and gate, combines reset signals from several sources to drive the zNEO reset pin.

One source is the debug/programming connector, J6. In normal operation the connector is empty and R9 keeps the reset inactive from this source.

The POR (Power on Reset) is generated by C71/C6. When power is applied C71 charges to a point where the input to U7 crosses the *input high* threshold and the zNEO is released from reset. The time constant is 10K * 10u which is around 100 milliseconds. R30 is used to provide a bit of hysteresis so the output of U7 doesn't oscillate through the transition region.

A finger friendly reset button, SW4, is provided to support programming and debugging. C70 provides a path to ground for stray RF.

3.6.2 Power Regulators

The unit may be supplied with a voltage that is compatible with the VR1 switch-mode regulator. Nominally a 6 cell pack would be used as this fits in the housing. 8 or 12 cell packs could also be used (two 9V rectangular batteries may also fit within the case).

VR2 steps the 5 volt rail down to 3.3V to supply the zNEO and other digital logic. This is an SOT23 package which has limited power dissipation capability. The current draw on the 3.3V rail is rather small.

D7 adds a diode drop to provide about 4.5V to the DRA818.

3.6.3 RF section

The RF section is the DRA818 transceiver module. All logic level control inputs are driven by the zNEO. Note that transmitting in not envisioned as there is no low-pass filter between the DRA818 and the antenna ports.

DV2, a PIN diode, provides antenna switching. With one of the diodes in DV2 forward biased, RF will pass through to the DRA818. With one of the diodes in DV2 reverse biased, RF is blocked. L1A and R5 keep the cathodes of DV2 near ground potential, providing a current path to ground. L2A/R6 and L3A/R7 RF isolate the MAX3188 drivers U6 and U11.

U5, the MAX870, is a switch capacitor voltage converter. This provides a -5V bias supply for U6 and U11. This reverse biases DV2 requiring almost no current, only the current required to charge capacitors during switching and a few micro amps of reverse leakage current.

U6 and U11 are bipolar drivers, i.e. RS232 drivers. When driving at +5V, the diode in DV2 is forward biased with current controlled by R5, R6 and R7. Target forward current is about 10mA. When driving at -5V, the diode in DV2 is reverse biased. Leakage current is in the micro-amp range.

Control of U6 and U11 is through pins PA2 and PA3 on the zNEO.

The PWMH0 signal may be used as a D/A converter. It is connected to the MIC input of the DRA818 (although we do not anticipate using it). R42/R49/L2/C62/C59/C60 form a low pass filter to remove the high frequency content from the PWM signal. C61 provides DC isolation for the DRA818.

The AF and SQ signals go off to the audio amplifier. SQ is also routed back to the zNEO to allow software to detect recognize when a signal is present.

3.6.4 TOY Clock

The DS1672 provides a binary Time-of-Year clock. BT1 provides power when the transmitter is switched off.

3.6.5 Audio

The audio from the DRA818 is buffered by U14. This is to lower the impedance of the signal that is routed to the volume control, R16. The range of the volume control adjustment is limited by R17 and R13.

The power amplifier is the U10, an LM4871. The SQ signal from the DRA818 is used to enable U10 only when there is an audio signal from the DRA818. This reduces the power consumption of the system when the DRA818 is not receiving a signal. When the DRA818 is receiving, its SQ signal is asserted low which enables U14 as well as the audio amplifier, U10. R4 limits the drive current from U1 allowing the zNEO to overdrive the SQ signal to force the received audio to be muted.

The zNEO may also generate and audio waveform using the PWM block present in the Z16F2811 (U1). The PWM signal is filtered and buffered by U15. This is the same MCP6273 rail-to-rail op-amp as U14. It is enabled by driving the TALK* signal low. This is Port B bit 2 in the zNEO. U13 combines the signals TALK* and SQ to drive the SHUTDOWN pin on the audio amplifier (U10). R17 and R36 from a summing junction to combine the two audio sources. The zNEO software may examine the state of the ZQ pin by configuring the bit as an input and it may configure as output to drive the pin.

J3 provides for an external speaker or headphones. It switches the internal speaker off when a plug is inserted.

3.6.6 FRAM/Flash

A single external memory device is provided to store configuration settings. Nominally an FRAM is used to simplify the driver.

3.6.7 Display

A simple 8 character 2 line LCD display is mounted on the main circuit board so that it can protrude through the case. It is controlled using the SPI interface. Clock and data are connected to the SPI function on the zNEO. Two additional controls make use of the PH2 and PH3 pins.

3.6.8 Network Port

A modified CI-V type interface is provided through J4. This port is not isolated as the unit is expected to be battery powered.

See the CI-V Implementation section 3.7 for details.

3.6.9 Digital Controls

Other than volume control, the unit has a single A rotary encoder with a button function provides primary control of the unit. The button function is a simple switch closure that takes the B_BTN signal to ground. The rotary encoder produces a two phase signal on B_CW and B_CCW that software must deal with.

These three signals are routed to two sets of pins on the zNEO. Pins on port G provide simple level reports on the signals. B_BTN also connects to PD7 which may be used to generate an edge triggered interrupt. B_CW and B_CCW are also connected to PA0 and PA1 which may be used to generate edge triggered interrupts.

3.7 CI-V Implementation

The CI-V implementation is essentially identical to that used on several previous projects. This particular implementation is not isolated assuming that the receiver will be battery powered when the CI-V port is in use.

Previous projects that were connected to external power supplies did make use of isolation. These projects were typically connected to high power transmitters. Here, we do not use the transmitter when the CI-V port is connected to a non-isolated driver.

3.7.1 Deviation from ICOM implementation

This implementation differs from the nominal ICOM implementation in that it is capable of full-duplex operation. Compatibility with the standard CI-V implementation is, however, trivial to achieve.

3.7.2 Implementation

U8 is the CI-V bus driver and U9 is the CI-V bus receiver. Both devices provide signal inversion to remain compatible with CI-V levels.

U8 is an open-drain(open collector) CMOS driver chip. The device (74LVC1G06) can drive up to 24mA and should be capable of driving several CI-V stations. A high value resistor, R34, is placed across the output of U8 to force the output to provide valid logic levels when testing.

U9 is a Schmitt-trigger inverter. The Schmitt-trigger is used to improve incoming signal quality. A 1K resistor appears on the incoming net to provide correct logic levels. The transmitting station would typically have a high-value resistor to maintain correct levels. The lower value resistor here provides some additional current to overcome noise. An RF bypass cap, C47, shorts any RF energy to ground to limit the noise seen at the input of U9.

3.7.3 CI-V Half Duplex Operation

Note that this half-duplex configuration may be used with a stereo plug on this end and and a mono plug on the far end with tip and ring connected together at either end.

Pins 1, 3 and 4 of JP1 are connected leaving the ring contact on the 3.5mm jack unconnected. A 3.5mm mono cable, the more-or-less normal CI-V cable, may then be used. Having pin 2 connected when using a mono cable usually shorts a signal to ground rendering the CI-V function inoperative.

3.7.4 CI-V Operation, mono/stereo cable

JP1-1 connects to JP1-2 and JP1-3 connects to JP1-4. The connecting cable, in this case, is a stereo 3.5mm at this end and a 3.5mm mono at the far end. Both tip and ring wires are connected to the tip terminal at the far end.

3.7.5 CI-V Operation, stereo/stereo cable

Pins 1, 3 and 4 of JP1 are connected leaving the ring contact on the 3.5mm jack unconnected. The connecting cable, in this case, is a stereo 3.5mm patch cord. This will only work with other KC0JFQ CI-V implementations.

3.7.6 Full Duplex Operation

JP1-1 connects to JP1-2 and JP1-3 connects to JP1-4. The connecting cable, in this case, is a stereo 3.5mm patch cord. This will only work with other KC0JFQ CI-V implementations. JP1 jumper block can be rotated 90 degrees to swap the TX and RX lines.

3.8 Power/Regulators

The unit nominally operates on a 6-cell battery pack. Either a 9V battery or six AAA cells in a holder.

Input voltage range is about 7V to 24V. Extended life is easily achieved using larger or more cells.

The input is protected against polarity reversal using a fuse and a reverse biased silicon diode. Hooking the battery up reversed will immediately vaporize the fuse. The fuse is a surface mount device which is slightly easier to replace than traces on the circuit board. The battery connector, once correctly wired to the battery holder, should prevent any battery polarity issues.

3.8.1 Rechargeable Battery

The circuit board has provision to add a charging jack to the receiver. When the power switch is in the off position the charging jack is connected to the battery. There is no current limiting in the path between the charge jack and the battery, this must be managed external to the circuit board.

3.8.2 VR1

The first stage regulator is a switch-mode device with a nominal efficiency of near 90amplifier. Given a switching frequency of several hundred kilohertz, switching noise should not be detectable in the audio.

3.8.3 VR2

The digital control is powered through VR2, a 3.3V linear regulator. This is a low noise device and the current requirements on the 3.3V rail are minimal.

3.8.4 D7

The RF module operated at approximately 4V. A rectifier diode is used to produce this drop from the 5V rail. A zener diode on the cathode of D7 keeps the maximum voltage on this rail at no more than 4.5V.

4 102-73718-10 Software Compatibility Issues

Refer to the page 6 of the schematic.

An attempt has been made to assign pins with similar functions to the same pins that are used on the 102-73718-10 fox transmitter to allow sharing of the codebase.

Several restrictions appear that limit this effort somewhat.
The control switch inputs must live on a port that that provides edge interrupts. This means that **B_BTN**, **B_CW** and **B_CCW** should all live on port-A or all on Port-D. We will try to move **B_CW** and **B_CCW** to Port-D and then move the contrast control **CONTR** to Timer-0 on Port-A. This will free up Timer-2 which is the system tick on the 102-73718-10 board.

5 Configuration

The *FOX DTOA Receiver* is controlled using the same zNEO processor that is used in the ICARC *FOX Transmitter*s. The *FOX DTOA Receiver* also has the same FRAM for storing configuration data. The command structure is similar, using 4 character mnemonics.

Following power-on (or reset) the zNEO scans the FRAM for configuration commands, looking for the the same record keys as used in the ICARC *FOX Transmitter*. Any initialization commands are executed in the order they are encountered in the file system.

6 Build Documents

The build documents are produced using *Eagle* V6.5.0.

All of these documents are produced using a combination of *Eagle* scripts, *Eagle* user language programs, and bash shell scripts.

6.1 Assembly

Start with the *Master Build Record* as a guide to assembling the board. Install the ceramic capacitors and the resistors first as these are relatively small and do not hinder access to the remaining parts.

Parts locations on the schematic and on the circuit board are listed in the *Master Build Record*. The schematic is a sheet.quadrant notation and the circuit board locations are from the *Pick & Place Zero Point* shown on the *PWB* (Printed Wiring Board) drawing. Note that the dimensions are taken from the top, so reverese direction on the bottom.

6.2 Schematics

Most logic gates have their power pins represented on a separate symbol to reduce clutter around the pins of the logic gate. The power symbol is a bit elaborate looking to force, as much as possible, the power pins to be connected to the correct rails following a rotation or mirroring operation.

You will also note that **no** schematic symbols are arranged to look like their packaging. The schematic should **not** represent the board layout, that is not its function. The schematic provides the connection netlist for the circuit board.

The fist page of the schematic has some additional *clutter* around the title block. These simply document that various documentation artifacts appear on the circuit board drawing.

6.2.1 Schematic Page 1

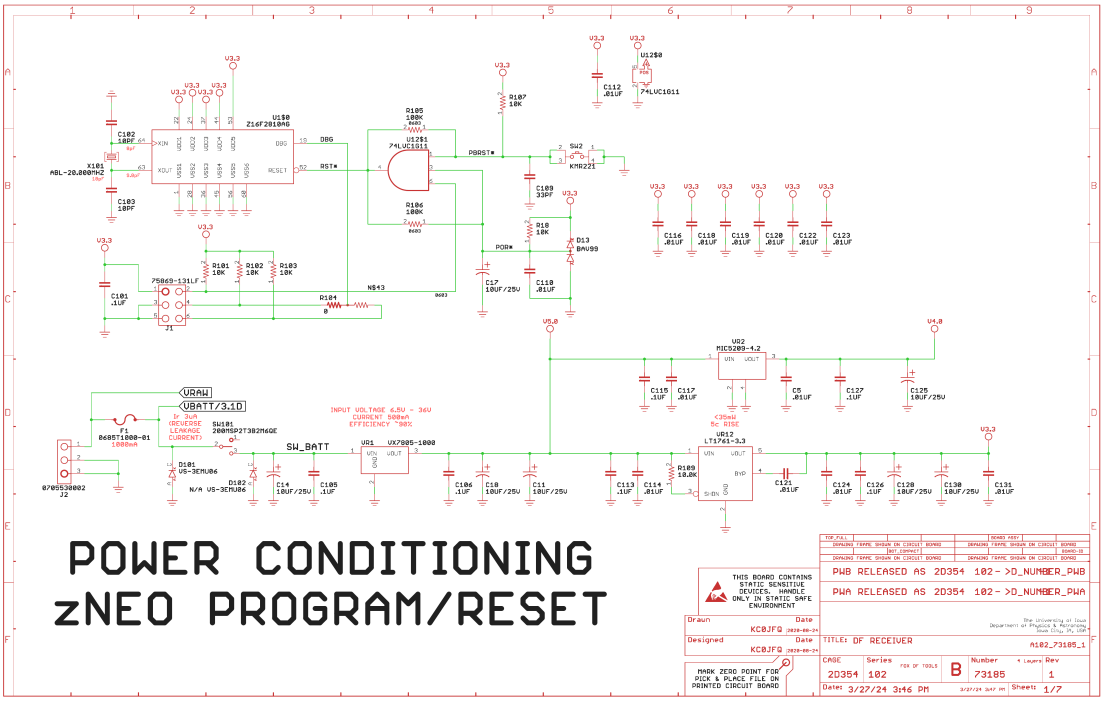

Figure 1: Page 1

Power supply uses a switch-mode regulator, VR1, in a 7805 package.

VR12 provides 3.3V for processor and logic.

VR2 provides 4.2V for the RF module.

U12 control reset to the zNEO.

J1 is the programming header.

6.2.2 Schematic Page 2

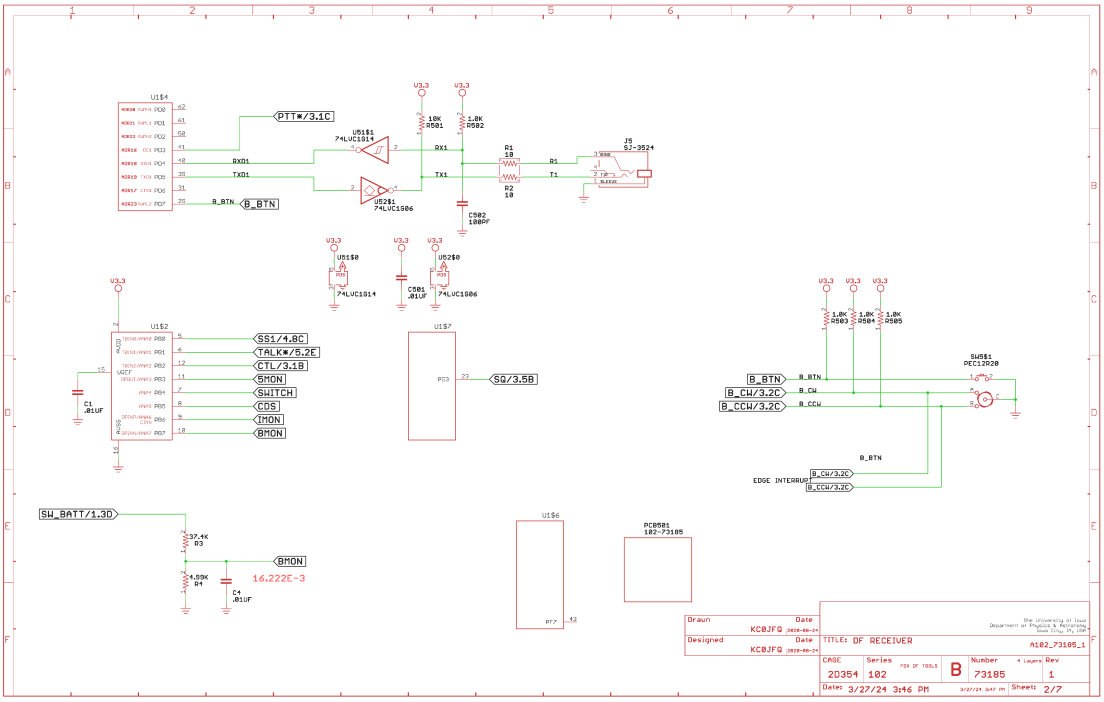

Figure 2: Page 2

U51 and U52 are the serial interface drivers. Use an FTDIchip TTL-232R-3V3-AJ cable to connect to a host system to configure.

Several signal nets connect to the zNEO on this sheet.

6.2.3 Schematic Page 3

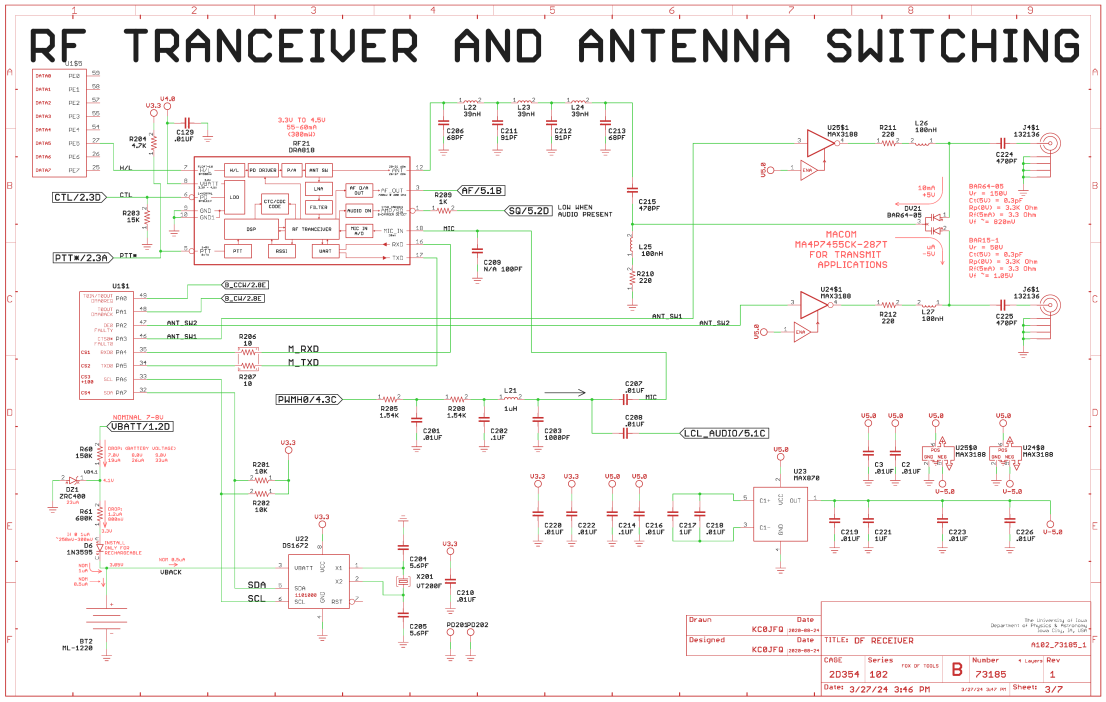

Figure 3: Page 3

RF21 is the RF module and U1 are the zNEO control pins.

U22, the DS1672 is the Time of Year clock.

U23 is a switch capacitor supply to provide a -5V bias for the antenna switching network.

U24 and U25 bias the PIN diode, DV21, to switch input between J4 and J6.

6.2.4 Schematic Page 4

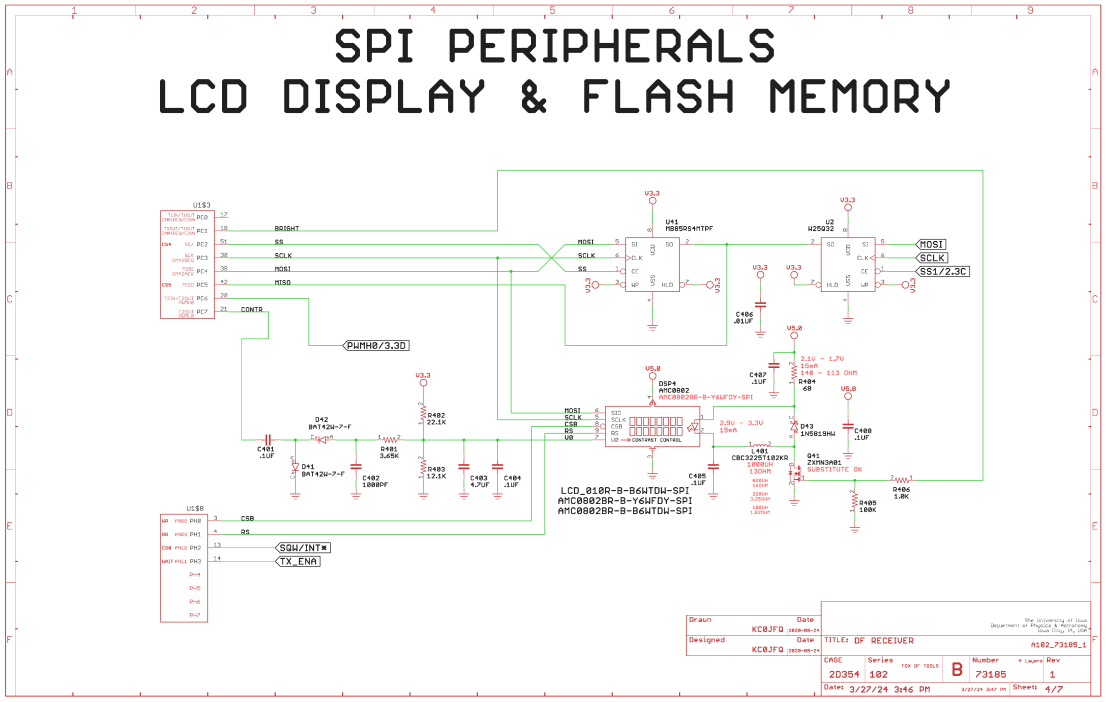

Figure 4: Page 4

U41 is the FRAM device. Nominally we install a 128Kb device to limit the cost of the device. Setup commands and sequencing commandsare stored here.

U2 is the FLASH device. Nominally we install an 8Mb device but larger devices can be substituted. Audio clips are stored in this device. stored here.

DSP4 is the LCD display. Pins 1 and 2 connect to a current controller that sets the display backlight brightness.

Pin 7 is the contrast control. The voltage applied to this pin varies between +3V and about -1V.

6.2.5 Schematic Page 5

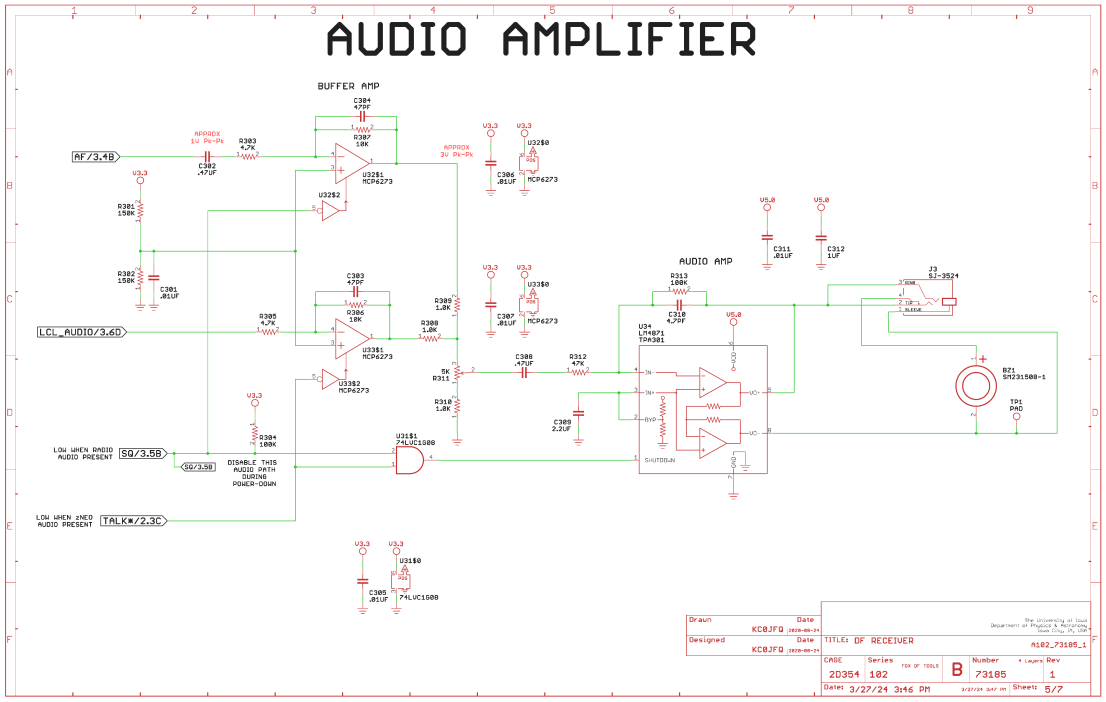

Figure 5: Page 5

This sheet has the audio switching circuits.

U34 is the audio amplifier. R312/R313 set the amplifier gain while R311 controls the input level to U34 (i.e. the volume control).

U32 and U33 are rail-to-rail op-amps with enable control. U32 connects audio from the RF receiver while U33 connects the DAC in the zNEO.

U31 logically ORs the enables from the DRA818 and zNEO. The zNEO may override the signal from the DRA818 to force the audio amplifier on.

6.2.6 Schematic Page 6

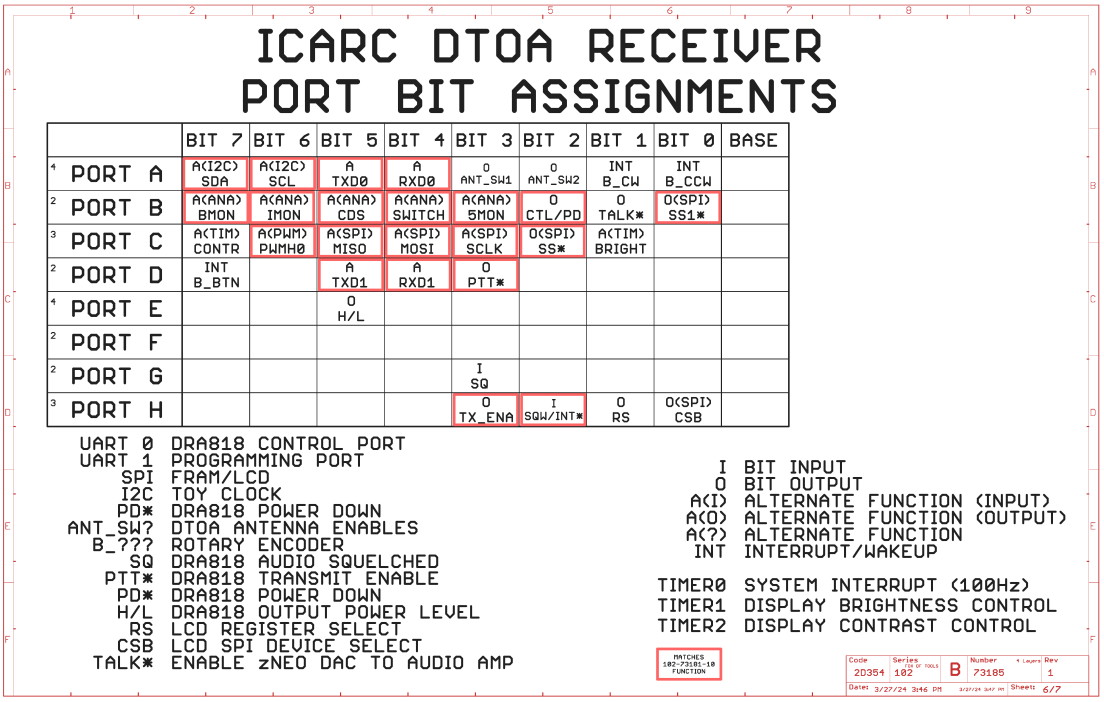

Figure 6: Page 6

zNEO pin assignment worksheet.

Pinout assignments attempt to match up with the 102-73181-10 fox transmitter to allow sharing of control modules.

6.2.7 Schematic Page 7

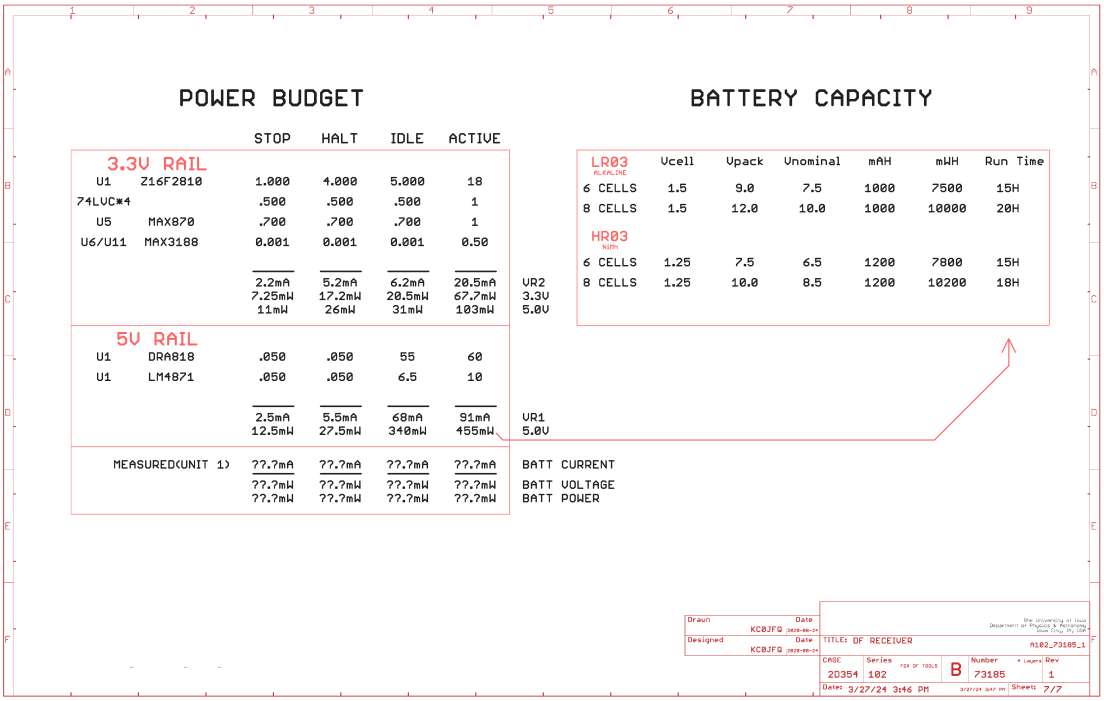

Figure 7: Page 7

Power calcualtions.

6.3 Printed Wiring Assembly drawings

This set of drawings have assembly notes and mechanical dimensions.

Assembly notes take care of mechanical issues that cannot be represented on the schematic.

The mechanical dimensions shown are needed to fit the assembled boards into an enclosure.

6.3.1 PWA top

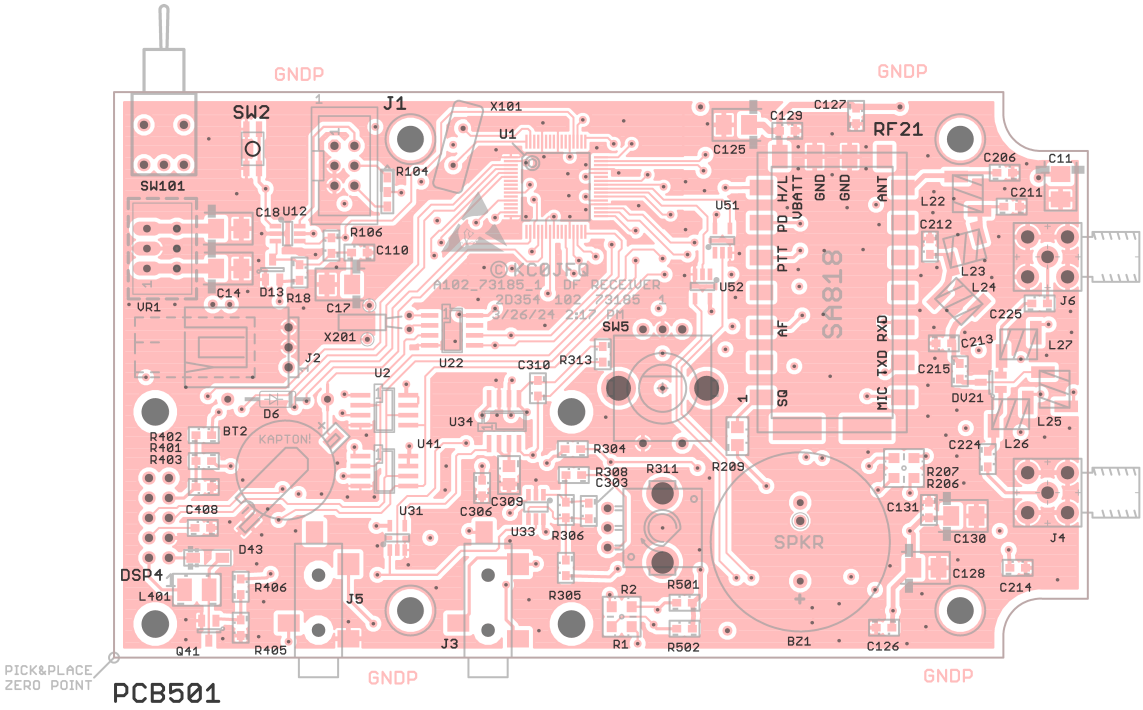

Figure 8: Top Copper

6.3.2 PWA bottom

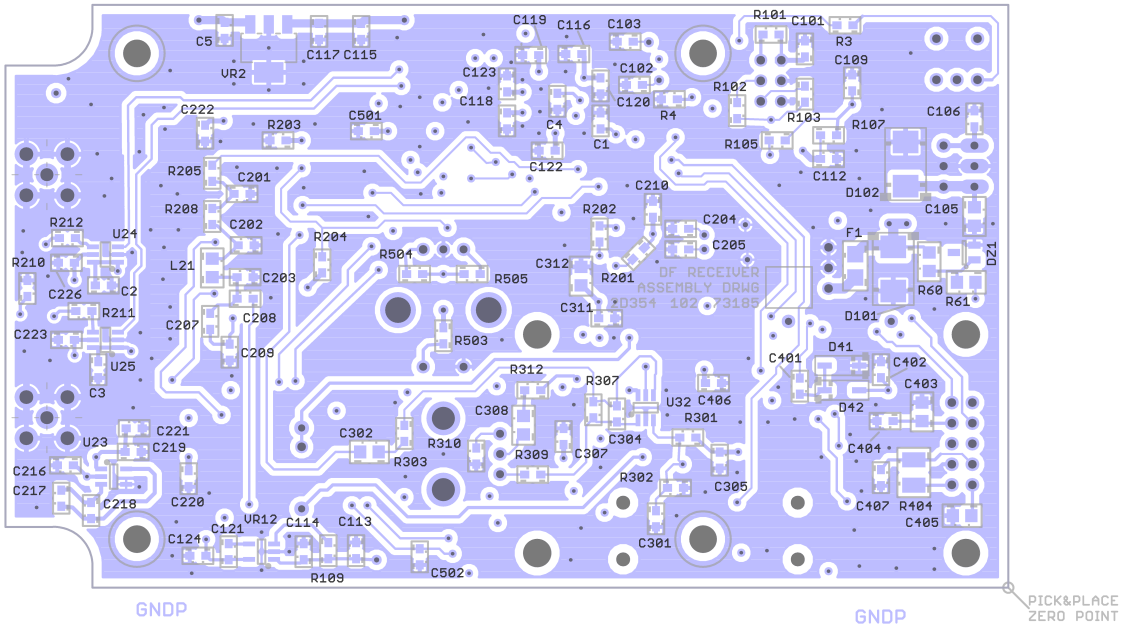

Figure 9: Bottom Copper

6.4 Parts Lists

The parts list included here is rendered from the HTML parts list. Some entries are color coded as indicated on the first sheet.

6.4.1 Parts List

Listing 1: packing.txt

```
Packing List FOX DF TOOLS DF RECEIVER                                    1
 (102-73185) derived from A102_73185_1.sch,  2024-03-26T14:18            2
    ↪ V2.58
 Idx   Qty   Part (Ref Des)          Value          Package              3
 ---   ---   ----------------       ------------   ----------           4
   6     1                BT2       ML-1220        BATT_ML1220          5
   7     1                BZ1       SM231508-1     SM231508             6
   8    37     C1 C110 C112          .01UF          SM0603               7
              C114 C116 C117                                            8
              C118 C119 C120                                            9
              C121 C122 C123                                            10
              C124 C129 C131                                            11
               C2 C201 C207                                             12
              C208 C210 C216                                            13
              C218 C219 C220                                            14
              C222 C223 C226                                            15
               C3 C301 C305                                             16
              C306 C307 C311                                            17
             C4 C406 C5 C501                                            18
   9    12    C101 C106 C113          .1UF           SM0603             19
              C115 C126 C127                                            20
              C202 C214 C401                                            21
              C404 C407 C408                                            22
  10     2         C105 C405          .1UF           SM0805             23
```

Listing 2: packing.txt-24

```
 ---   ---   - - - - - - - -  - - - - - - - -  - - - - - - - -          24
  11     2         C302 C308          .47UF          SM0805             25
  12     2         C203 C402          1000PF         SM0603             26
  13     1              C502          100PF          SM0603             27
  14     2         C102 C103          10PF           SM0603             28
  15     7    C11 C125 C128          10UF/25V       SMP_M3528          29
             C130 C14 C17                                               30
                   C18                                                  31
```

Listing 3: packing.txt-32

16	1	C312	1UF	SM0805
17	2	C217 C221	1UF	SM0603
18	1	C309	2.2UF	SM0805
19	1	C109	33PF	SM0603
20	1	C310	4.7PF	SM0603

Listing 4: packing.txt-38

21	1	C403	4.7UF	SM0805
22	3	C215 C224 C225	470PF	SM0603
23	2	C303 C304	47PF	SM0603
24	2	C204 C205	5.6PF	SM0603
25	2	C206 C213	68PF	SM0603

Listing 5: packing.txt-44

26	2	C211 C212	91PF	SM0603
27	1	C209	N/A 100PF	SM0603
28	1	D6	1N3595	DO35-050
29	1	D43	1N5819HW	SOD123FL
30	1	DSP4	AMC0802	AMC0802B

Listing 6: packing.txt-50

31	1	DV21	BAR64-05	SOT23-3
32	2	D41 D42	BAT42W-7-F	SOD123
33	1	D13	BAV99	SOT23-3
34	1	D102	N/A VS-3EMU06	DO214AC
35	1	D101	VS-3EMU06	DO214AC

Listing 7: packing.txt-56

36	1	DZ1	ZRC400	SOT23-3
38	1	F1	0685T1000-01	SM1206
39	1	J2	0705530002	HDR_50-57-9403
40	2	J4 J6	132136	SMA_04A
41	1	J1	75869-131LF	HDR_2X3

Listing 8: packing.txt-62

42	2	J3 J5	SJ−3524	SJ−352X	
43	3	L25 L26 L27	100nH	AIAC−1812	
44	1	L21	1uH	SM0805	
45	3	L22 L23 L24	39nH	AIAC−1812	
46	1	L401	CBC3225T102KR	SM1210	

Listing 9: packing.txt-68

47	1	PCB501	102−73185	HAMMOND_1599EBAT	
51	1	Q41	ZXMN3A01	SOT23−3	
52	1	R104	0	SM0603−3	
53	8	R308 R309 R310	1.0K	SM0603	
		R406 R502 R503			
		R504 R505			
54	2	R205 R208	1.54K	SM0603	

Listing 10: packing.txt-76

55	1	R109	10.0K	SM0603	
56	5	R105 R106 R304	100K	SM0603	
		R313 R405			
57	10	R101 R102 R103	10K	SM0603	
		R107 R18 R201			
		R202 R306 R307			
		R501			
58	4	R1 R2 R206 R207	10	SMR0805−41	
59	1	R403	12.1K	SM0603	

Listing 11: packing.txt-86w

60	1	R60	150K	SM0805	
61	2	R301 R302	150K	SM0603	
62	1	R203	15K	SM0603	
63	1	R209	1K	SM0805	
64	1	R402	22.1K	SM0603	

Listing 12: packing.txt-92

65	3	R210 R211 R212	220	SM0603	93
66	1	R401	3.65K	SM0603	94
67	1	R3	37.4K	SM0603	95
68	3	R204 R303 R305	4.7K	SM0603	96
69	1	R4	4.99K	SM0603	97

Listing 13: packing.txt-98

70	1	R312	47K	SM0603	99
71	1	R311	5K	PTV09A-4	100
72	1	R61	680K	SM0805	101
73	1	R404	68	SM1210	102
74	1	RF21	DRA818	SA818	103

Listing 14: packing.txt-104

75	1	SW101	200MSP2T3B2M6QE	SW_200_M6	105
76	1	SW2	KMR221	SW_KMR2	106
77	1	SW5	PEC12R20	SW_PEC12R2	107
79	1	U52	74LVC1G06	SOT23-5	108
80	1	U31	74LVC1G08	SOT23-5	109

Listing 15: packing.txt-110

81	1	U12	74LVC1G11	SOT23-6	111
82	1	U51	74LVC1G14	SOT23-5	112
84	1	U22	DS1672	SO8	113
85	1	U34	LM4871	SO8	114
86	2	U24 U25	MAX3188	SOT23-6	115

Listing 16: packing.txt-116

87	1	U23	MAX870	SOT23-5	117
88	1	U41	MB85RS4MTPF	SO8_209	118
89	2	U32 U33	MCP6273	SOT23-6	119
90	1	U2	W25Q32	SO8_209	120
91	1	U1	Z16F2810AG	LQFP64UI	121

Listing 17: packing.txt-122

92	1	VR12	LT1761−3.3	SOT23−5	123
93	1	VR2	MIC5209−4.2	SOT223	124
94	1	VR1	VX7805−1000	TO220−3/VX78	125
95	1	X101	ABL−20.000MHZ	HC49U	126
96	1	X201	VT200F	X–CFS206	127

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6.5 Parts Substitution Notes

Parts selection notes.

6.5.1 D101/D102

D101 is populated assuming that the reverse leakage current is less than the self discharge current of the battery. If the selected diode is leaky, populate it in the D102 position.

The D101 position is the preferred position as this will give immediate feedback should the battery be connected backwards.

6.5.2 D14

D14 is selected for forward voltage drop of at least 700mV when only a few mA of current are passing through the device.

Devices with less forward voltage drop can lead to stressing the DRA818/SA818 during shutdown when little current is flowing through D14.

6.5.3 DV21

No special requirements for the PIN diode, substitute as needed.

6.5.4 DS1672

System operation does not depend on this device being present.

6.5.5 BZ1

The PCB layout directly accommodates the SM231508-1 speaker. Substitute a CVS-1508 if desired using the additional hold near the - terminal for the SM231508-1 pad.

6.5.6 zz

6.5.7 zz