ICARC Fox TDOA Tracker

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This is the start of a manual for the ICARC FOX TDOA Tracker. It covers the 102-73174-51, 102-73174-71, 102-73174-82, 102-73174-91 and 102-73174-97 boards.

It is a work-in-progress right now so suggestion for updates may be sent to **kc0jfq@n952.ooguy.com**.

Full size documents may be found here: http://n952.ooguy.com/HamRDF

LaTeX Source Files:

1.		//home/wtr/Fox_TDOA_zNEO/trunk/Fox_zNEO_TDOA.tex
2.	1	//home/wtr/Fox_TDOA_zNEO/trunk/FOX_zNEO_TDOA_Glossary.tex
3.	3	//home/wtr/Fox_TDOA_zNEO/trunk/FOX_zNEO_TDOA_Motivation.tex
4.	5	//home/wtr/Fox_TDOA_zNEO/trunk/FOX_zNEO_TDOA_Revision_History.tex
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Chapter 1

Glossary of Terms

Source File: FOX_zNEO_Glossary.tex

There is an attempt being made to use some terms in this document in a precise manner. Some of the discussions become a bit muddled when terms are used casually.

1.1 FLASH

An in-circuit erasable and programmable memory.

A type of non-volatile memory that exhibits very asymmetric access speed. Write speed is several orders of magnitude slower that read speed.

Update is handled by erasing the entire device and then loading it one (32 byte) record at a time.

1.2 FRAM

Ferro Magnetic **R**andom **A**ccess **M**emory.

A type of non-volatile memory that exhibits symmetric access speed. In other words the write speed is the same as the read speed. The type of memory is byte accessible (for both read and write) as well as non-volatile.

Update may be handled a record at a time or by erasing the entire device.

1.3 ISR

Interrupt Service Routine.

This is a block of code that deals with an even that is not triggered by the normal flow of instructions in the processor.
Examples would be incoming serial traffic or a timer event.

1.4 Processor

This refers to the zNEO system-on-chip. It has an instruction execution engine (i.e. the CPU), program memory, data memory, and a variety of peripherals.

1.5 Program

71 This refers to the code in the zNEO system-on-chip.

1.6 Sequence

We will use the term **SEQUENCE** in this document to describe a set of (FRAM) instructions
82 that are executed as a group.

Typically this *sequence* is stored in external FRAM memory.

1.7 xxx

187 xxx (the $24^{\text{th.}}$ letter of the alphabet)

Chapter 2

Motivation

Source File: FOX_zNEO_Motivation.tex

Why ?

Explore an automated direction finding machine.

2.1 Requirements

These are required for operation and remain unchanged from the 102-73161 series boards.

2.1.1 2M Band

This

2.1.2 Battery Operation

We

2.1.3 Physical Size

Lets keep it in the standard Hammond 1599E enclosure.

2.1.4 Programmable without special tools

Same as the FOX Transmitter.

2.2 Desirements

These are desired features

Chapter 3

Revision History

Source File: FOX_zNEO_Revision_History.tex

List of updates to the hardware and software.

3.1 Software

Updates and changes to the Operating Software

3.1.1 V0.01

Initial Release.

Chapter 4

14

Theory of Operation

Source File: FOX_zNEO_Theory_Operation.tex

The tracker is composed of several units and may be configured in multiple ways.

4.1 zNEO main board

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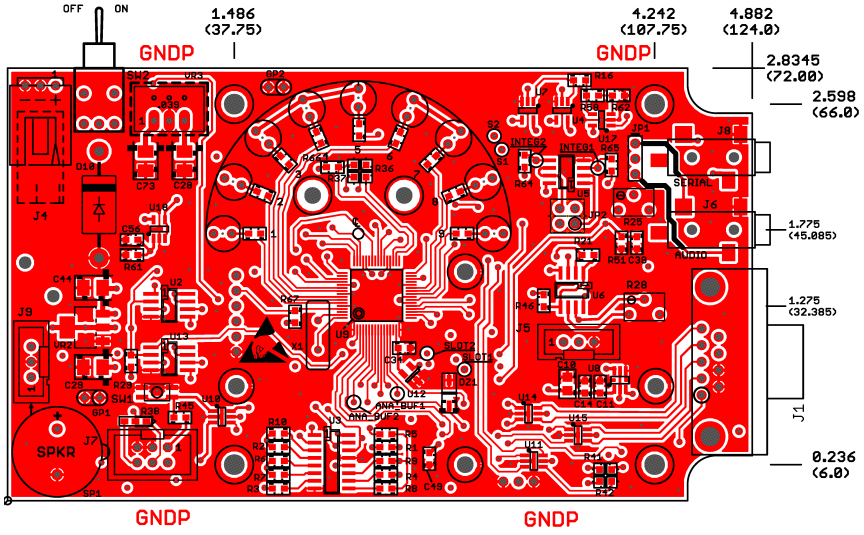

Figure 4.1: 1st. generation TDOA Tracker (102-73174-50)

The processing element is the same zNEO chip that is used on the Fox Transmitter system. Much of the software is reused from that project.

4.1.1 Compass Display

Nine LEDs form a meter or compass display. This is directly controlled by the zNEO using the PE and PG pins. Software determines if it acts as a compass display or as a meter display.

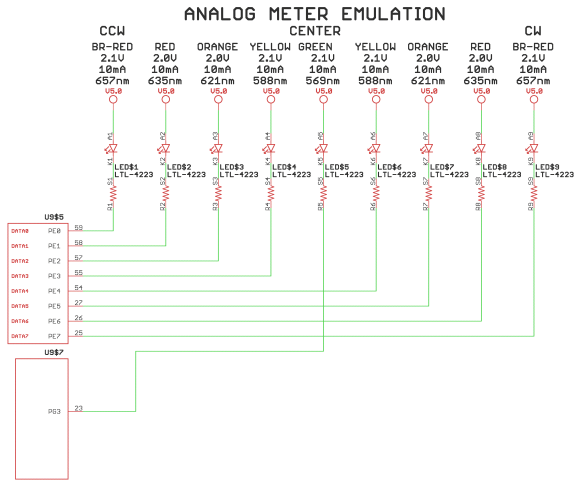

Figure 4.2: Display Logic

The display driver is straight-forward, we simply connect Port E and Port G pins to the LED array.

4.1.2 Antenna Control Interface

The antennas control interface is simply a set of 4 digital pins that select one of the nine antennas controlled by the antenna controller.

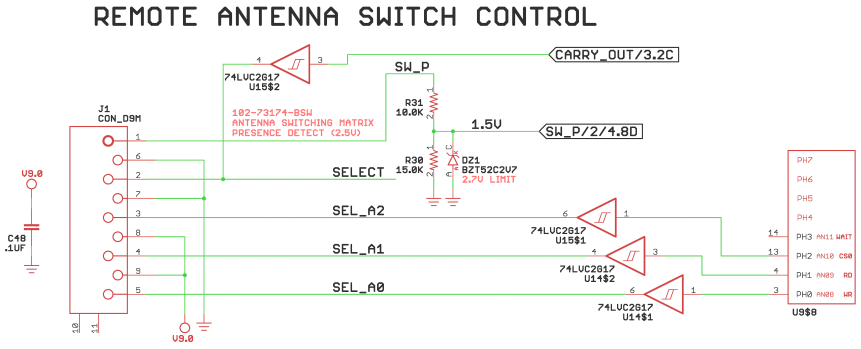

Figure 4.3: Antenna Control Logic

To drive the antenna select, we simply buffer three select lines from the zNEO. The **SELECT** net is driven by a logic gate.

4.1.3 Daughtercard Interface

The daughtercard interface occurs through two vertical connectors.

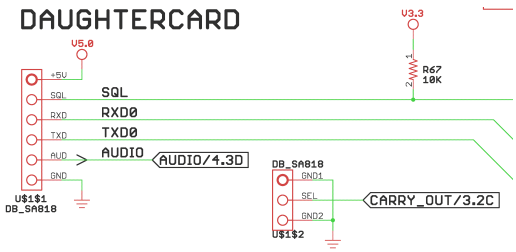

Figure 4.4: Daughtercard Control Logic

The signal interface to the daughtercrd is quite simple.

SQL from SA818 on daughtercard

The carrier detect signal from the SA818 tranceiver. This line is HI when detecting carrier energy.

RXD0 from SA818 on daughtercard

The serial data (i.e. status) from the SA818.

This datapath uses the same port to control the SA818 as does the Fox Transmitter to allow use of the same serial handler.

TXD0 to SA818 on daughtercard

The serial data (i.e. commands) to the SA818.

The datapath matches Fox Transmitter here too.

AUDIO from SA818 on daughtercard

The audio data from the SA818.

CARRY_OUT to antenna switch on daughtercard

Control/timing for the antenna switch on the daughtercard.

Power and Ground for the SA818 on the daughtercard

Note that we call out the SA818 from Nice-RF (and not the DRA818 form Dorji).

The datasheet indicates that the SA818 module will run on 5V.

4.1.4 Host Configuration Interface

This is the same serial interface as seen on the Fox Transmitter to allow configuring the system.

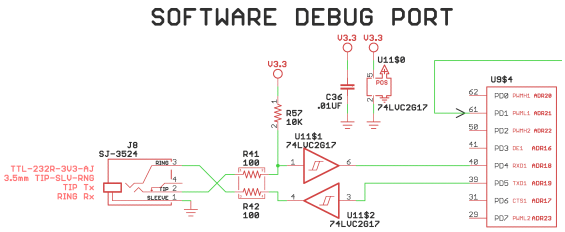

Figure 4.5: Host Configuration Port

4.2 Synchronous Detector

Source File: FOX_zNEO_Theory_Operation_2.tex

This section will discuss the detector logic.

Much of the design is based on a description posted by KA7OEI (https://ka7oei.blogspot.com/2016/11/tdoa-direction-finder-systems-part-1.html).

This function resides on the main board but has been broken out into its own section to make the TOC easier to navigate.

4.2.1 Clock Generator

Master clock generator circuit.

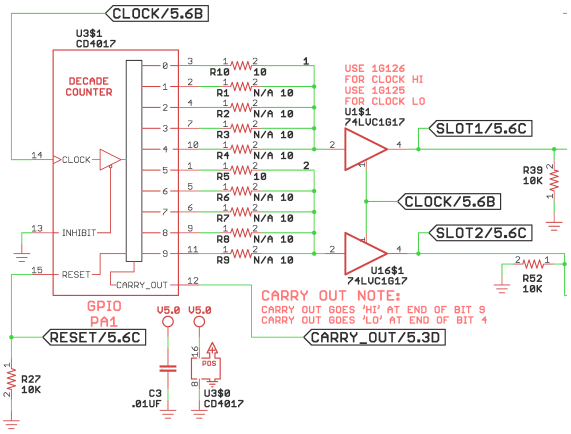

Figure 4.6: B series CMOS Clock Generator

The zNEO uses one of its timers to generate the reference clock supplied on the **CLOCK** net. This is nominally set to 1KHz. The zNEO also controls the **RESET** net.

The CD4017 generates a series of pulses on its ten output pins. Two of the ten are selected to produce the **SLOT1** net and the **SLOT2** net.

The **carry out** from the CD4017 is a aquare ware that drives the antenna switch by selecting between the center element and one of the edge elements, see figure 4.6 on page 12.

The **CARRY_OUT** net is supplied to an input pin on the zNEO so that the current state can be monitored.

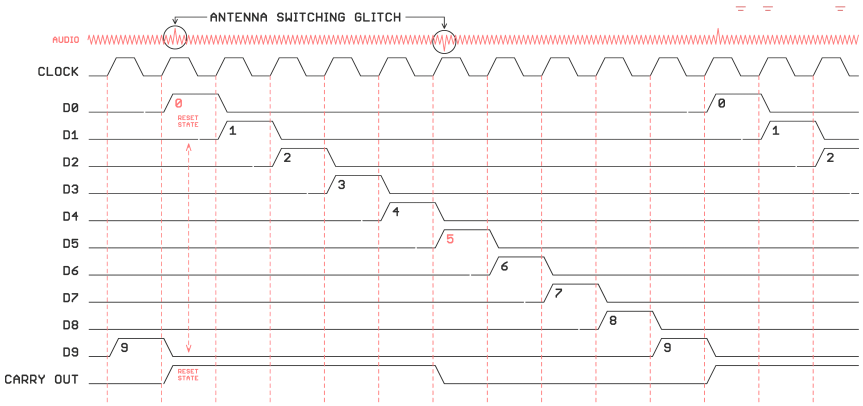

Figure 4.7: Clock Waveform

This is the waveform we expect out of the CD4017.

Note that U1 and U16 sit between the CD4017 and the **SLOT*** nets. The part number on the drawing is for a non-inverting buffer, which has no effect on the net. The net can be gated with the **CLOCK** net to reduce the sampling time to the integrator. This gating is accomplished by using a tri-state buffer (in the U1 and U16 position) to shrink the sampling period to ½ clock cycle. Use a 74LVC1G126 to select the first half and a 74LVC1G125 to select the second half.

.

4.2.2 Audio Chopper

The audio chopper circuit samples audio data for analysis.

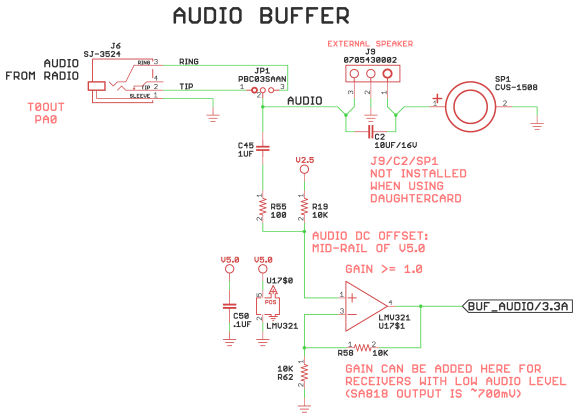

Figure 4.8: Audio input circuit

Audio is taken from the receiver, if external through a 3.5mm jack. Using the internal receiver, J6 is not populated and the audio from the internal source is through the **AUDIO** net.

C45/R19/R15 remove any DC offset from the audio, centering it around 2.5V (half the supply rail).

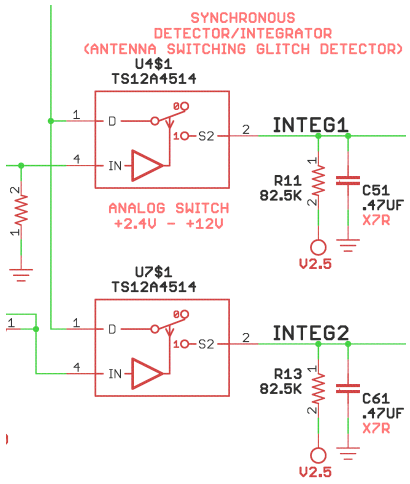

Figure 4.9: Audio chopper circuit

The **SLOT1** and **SLOT2** signals pass audio from the receiver through to a crude integrator. U4 and U7 take the average of the waveform from the radio during **SLOT1** and **SLOT2** and stores the average value on C51 and C61. R11 and R13 allow the integration to decay between sampling periods. See the timing diagram in figure 4.7 on page 13.

The **SLOT1** and **SLOT2** nets are provided to the zNEO so the current system state can be determined.

.

4.2.3 Disintegrator

Sounds catchy?

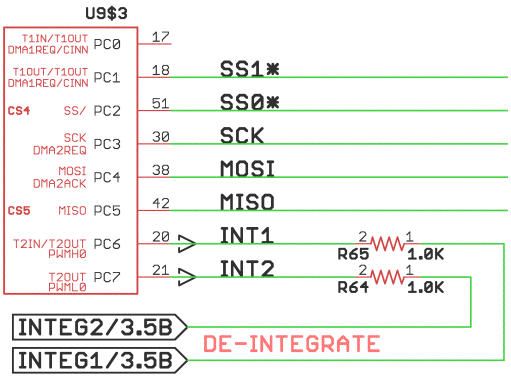

Figure 4.10: De-integrator

These two pins on the zNEO may be used to clear the integrator nets (**INTEG1** and **INTEG2**) to either 0V or 3.3V.

Clearing to 0V is, perhaps, the simplest case. Here we configure the pin to be open-drain and drive it to logic zero to discharge C51 and C61.

Clearing to 3.3V is a bit more involved in that the output data register is loaded with a '1' and then the data direction register is switched between input and output. The value of R64 and R65 may need to be changed for the clear operation to have the desired effect.

You are, of course, free to treat **INTEG1** and **INTEG2** differently if needed.

4.2.4 Bias Buffer

Mid-rail bias for audio processing.

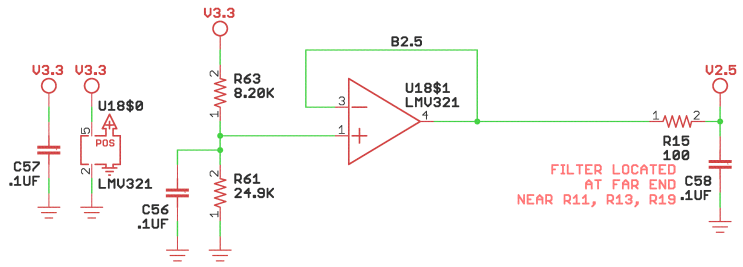

Figure 4.11: Bias Buffer

This voltage is used to de-integrate the **INTEG1** and **INTEG2** nets toward a *no signal* state.

This also provides a DC level for the incoming audio signal in section 4.8 on page 14.

4.2.5 Buffer Amp

Isolate the integrator from downstream stages.

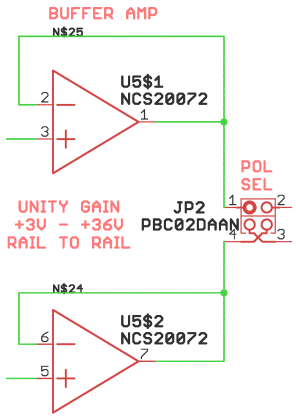

Figure 4.12: OP-Amp Follower

All we do here is present a high impedance to the integrator and a low-impedance to the downstream circuits.

The JP2 jumper array provides a means of swapping the two antenna samples. This provides the capability to always drive the meter in the positive direction.

This will be receiver dependant.

4.2.6 Differential Amplifier

The Differential Amplifier is powered from both a +5V and a -5V rail.

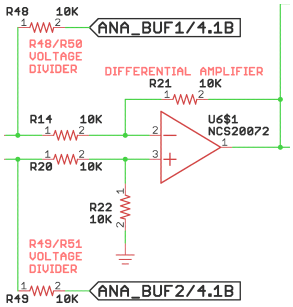

Figure 4.13: Differential amplifier circuit

Now we difference the integrated offsets in the audio signal.

The **ANA_BUF1** and **ANA_BUF2** nets are also sent directly to the zNEO A/D.

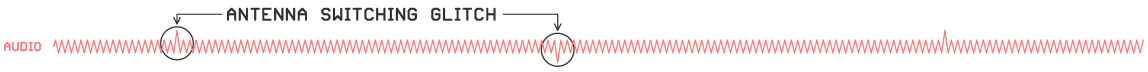

Figure 4.14: Nominal Audio Waveform

With the antenna pair not pointing normal to the transmitter, we expect to get something like the above waveform on the **AUDIO** net. We then attempt to isolate these glitches, caused by our antenna switching, using the U4/U7 switch.
Observe in ficure 4.7 on page 13 that **U3/D0** and **U3/D5** pass the waveform through to the integrator as the antenna element is switched.
.

4.2.7 Offset adjust

U6$1 from the previous stage may well produce a negative voltage, which can be rectified using JP2. U6$1 may also produce a voltage that is out-of-range for a mechanical meter or out-of-range of the zNEO A/D. The gain and offset may be corrected using U6$2.

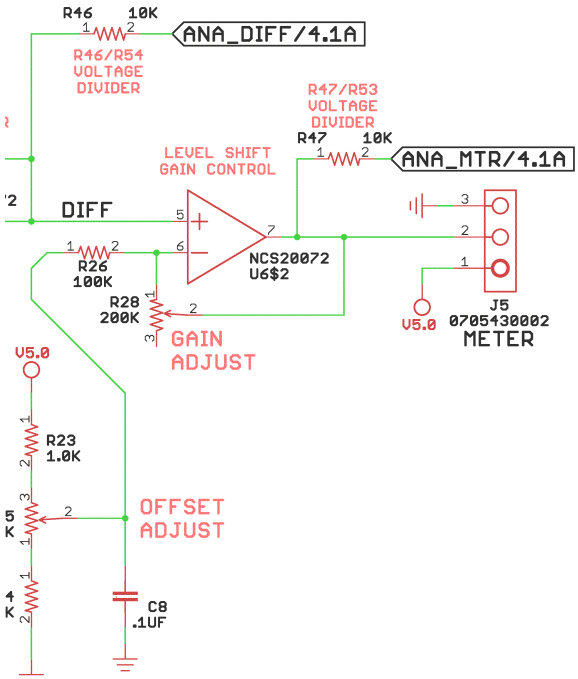

Figure 4.15: Offset adjust

A voltmetxer may be directly attached to J5 to see a real time indication of the difference signal seen by the synchronous detector. This **ANA_MTR** net is also sent to the zNEO A/D section.

4.2.8 zNEO port pin assignments

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
102-73174-51	PORT A	ANT_DR	NOT USED	TXD0	RXD0	SLOT2	SLOT1	RESET	CLOCK
102-73174-51	PORT B	BMON	IMON	ANA_MTR	ANA_DIFF	5MON	ANA_BUF1	ANA_BUF2	SW_P
102-73174-51	PORT C	INTEG2	INTEG1	MISO	MOSI	SCLK	SS0*	SS1*	NOT USED
102-73174-51	PORT D	NOT USED	NOT USED	TXD1	RXD1	NOT USED	NOT USED	SQL	NOT USED
102-73174-51	PORT E	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1
102-73174-51	PORT F	NOT USED	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
102-73174-51	PORT G	NO PIN	NO PIN	NO PIN	LED9	NO PIN	NO PIN VCMO_EN*	NO PIN	NO PIN
102-73174-51	PORT H	NO PIN	NO PIN	NO PIN	NO PIN	NOT USED	SEL_A2	SEL_A1	SEL_A0

Figure 4.16: zNEO port pin assignments

4.3 Antenna Rotator

Source File: FOX_zNEO_Theory_Operation_3.tex

This the the antenna switching matrix.

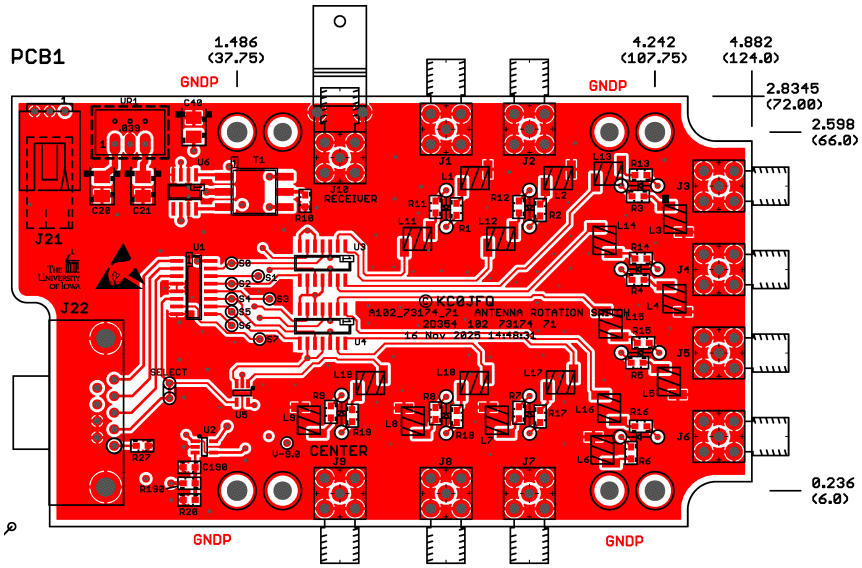

Figure 4.17: 1st. generation TDOA Rotator (102-73174-71)

The system assumes a semicircular array of eight radial antennas and one center antenna. This circuit board is used to electrically rotate an antenna array by switching between a common antenna element and one of eight radial elements.

4.3.1 Diode Switching

The RF switch.

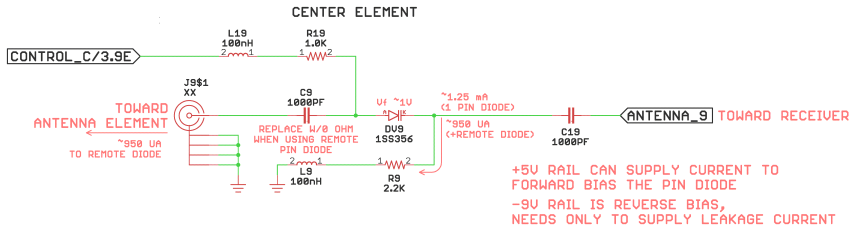

Figure 4.18: Diode Switching

The switching diode acts as an RF switch.

When forward biased, the diode acts much like a low-value resistor to the incoming RF signal. When reverse biased, the diode acts much like a low-value capacitor to the incoming RF signal.

The capacitors provide DC isolation, allowing only the RF signal to pass.

The capacitor leading to the antenna element may be replaced with a 0Ω resistor when using the 102-73170-32 *PIN Diode Antenna Base*. The 102-73170-32 board is also fitted with the same PIN Diode and ground bias to allow additional isolation.

4.3.2 Diode Bias Calculations

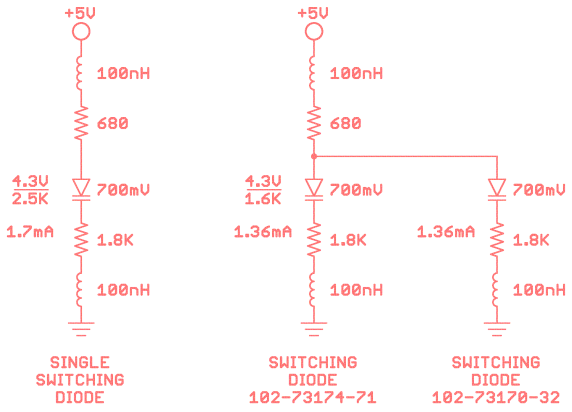

Figure 4.19: Diode Bias Calculations

On the left is the nominal configuration when using only the switching matrix on the 102-73174-71 circuit board. Here a single PIN diode is used as the RF switch. Calculated forward current is, as shown, about 1¾ milliamp.

On the right is shown with the 102-73170-32 board populated with a second PIN diode to further improve isolation inthe system. The additional diode electrically appears as shown on the right side. The overall current through the two diodes rises but this individual currents drops a bit to about 1⅓ milliamp.

Reverse bias, requiring very little current, will be at the negative rail esentially unaffected by the resistors. The +5V end of the diode circuit is biased at around -9V to shut the diode off.

4.3.3 Diode Bias

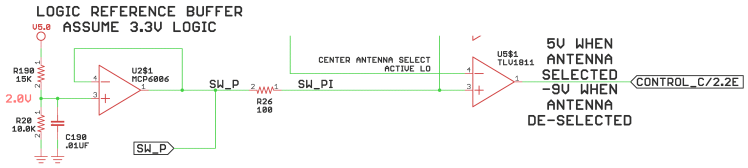

Figure 4.20: Diode Bias

The switching bias is produced using a comparator that is powered from 5V and -9V. The digital control is 5V logic which is routed to the - input of the TLV1811. The + input of the TLV1811 comes from a buffered voltage divider that is set to approximatley 2V.

The TLV1811/TLV1814 are all powered from +5V an -9V accounting to provide a convenient biasing scheme for the PIN diodes.

4.3.4 Antenna Decode

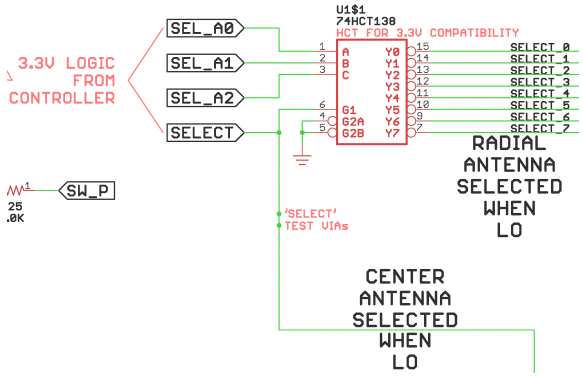

Figure 4.21: Antenna Select

The host controller (see section 4.1 on page 8) supplies the four select signals to the 74HC138.

4.3.5 Antenna Control Timing

Target timing to the antenna switch.

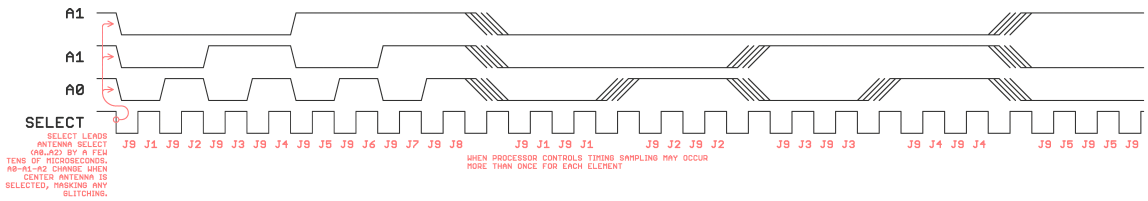

Figure 4.22: Antenna Control Timing

The hardware (i.e. the CD4017) generates the **SELECT** net with a 50% duty cycle.

The processor on the main board is then responsible for driving the 3 select lines (A2..A0) to the 3:8 decoder. Although figure 4.22 shows A2..A0 being synchronous with the **SELECT** net, in practice the zNEO may sample multiple times before changing the A2..A0 nets to the next antenna.

When the **SELECT** net is **hi** one of the eight radial antennas is selected. When the **SELECT** net is **lo** the center antenna is selected.

The controller electronically rotated the array by switching between the center element and one of the radials. The audio signal can then be measured and the controller can rotate on to the next antenna element.

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4.3.6 Antenna Array

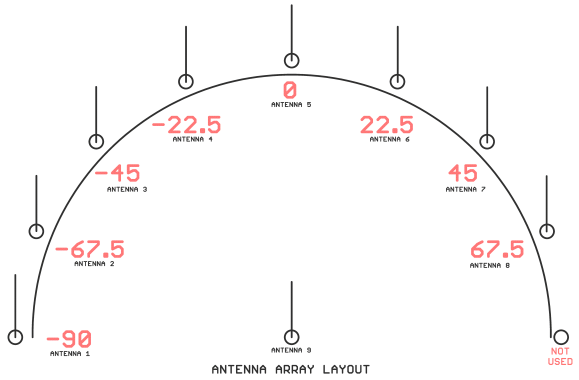

Figure 4.23: Antenna Array

Here is a suggested layout for an eight + one antenna array. This gives us the ability to rotate the array through 360°in 22.5°increments.

The operating software in the 102-73174-52 control board is then free to synthesize almost any pattern.

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4.4 SA818 Receiver

Source File: FOX_zNEO_Theory_Operation_4.tex

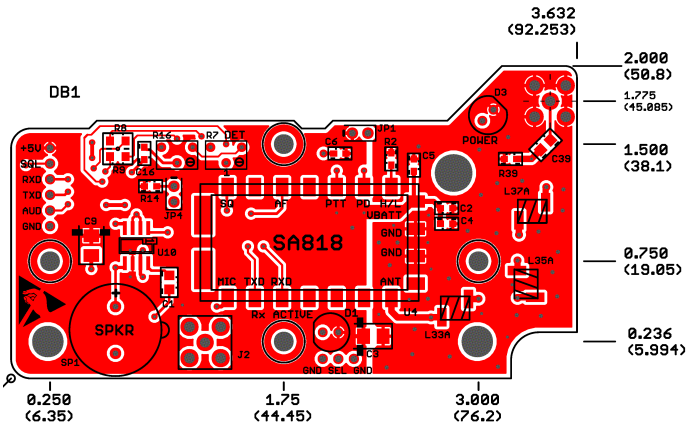

Figure 4.24: 1st. generation TDOA Receiver (102-73174-90)

This receiver board requires the antenna switch (102-73174-71).

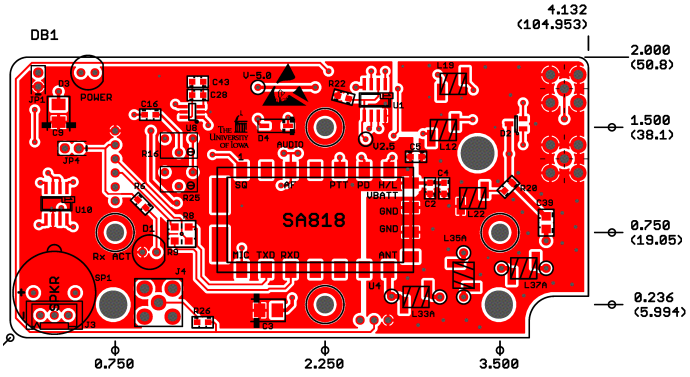

Figure 4.25: 2nd. generation TDOA Receiver (102-73174-97)

This receiver board may be used stand-alone with two antennas or with the antenna switch (102-73174-71).

4.4.1 Receive-only configuration

The receiver section performs the function of a handheld tranceiver. All that is required of the receiver is to listen to the Fox Transmitter and pass the audio back to the synchronous detector.

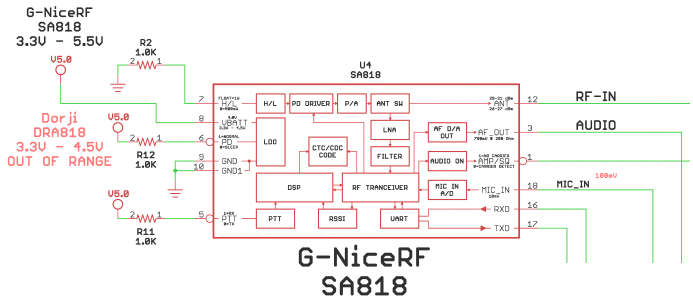

Figure 4.26: SA818 Receiver

The receiver is strapped into a **receive only** mode of operation. There is no mechanism to place the SA818 into a low power mode, it is always listening for radio traffic on the selected frequency. The carrier detect line is passed back to the main board to allow the zNEO to determine when radio traffic in present.

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4.4.2 Low Pass Filter

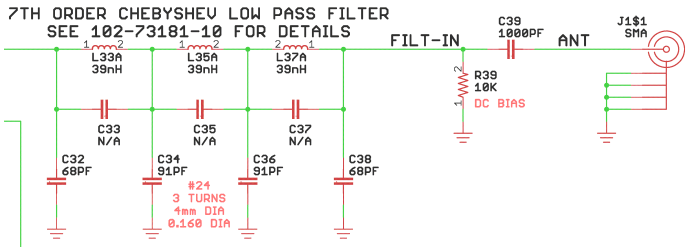

Figure 4.27: Low Pass Filter

The SA818 requires an external low pass filter to supress transmit harmonics. We copy the filter topology from the Fox Transmitter to suppress any out-of-band energy.

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4.4.3 Audio Amplifier

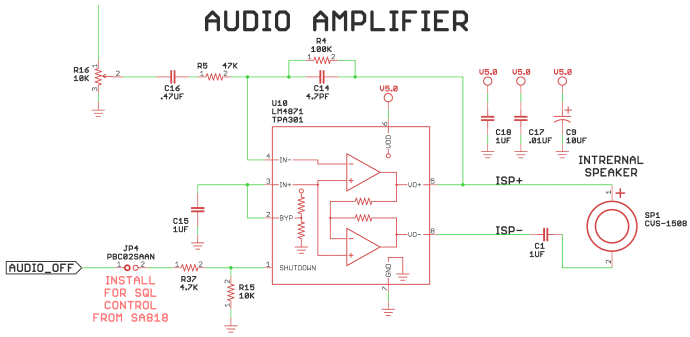


Figure 4.28: Audio Amplifier

We add a minimal audio amplifier to drive a speaker.

Not very loud!

4.4.4 Main Board Interconnecst

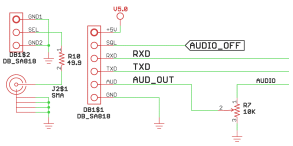


Figure 4.29: Main Board Interconnecst

Power, Ground and signals to and from the main board.

AUDIO_OFF

Status signal from the SA818 that indicates when there is no carrier present.

AUD_

Demopdulated audio from the SA818.

RXD

Serial data from the command interface of the SA818.

TXD

Serial data to the command interface of the SA818.

4.4.5 Antenna Switch

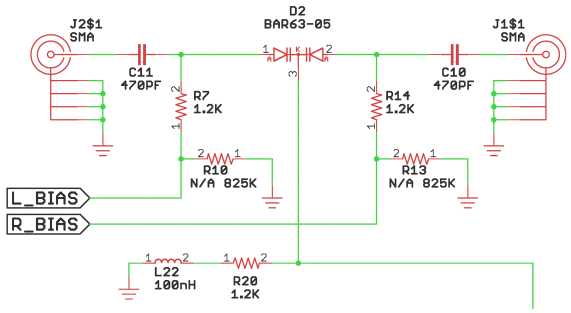


Figure 4.30: Antenna Switch

The antenna switch is borrowed (somewhat) from the 102-73170-20 design with minor changes. Note that R10/R13 are on the *more isolated* side of R7/R14 and are no longer necessary. This location keeps this ground reference off of the RF path between antennas and radio.

This drawing is from the 102-73174-97 update which reworks the PIN diode drive to match the 102-73174-71 model.

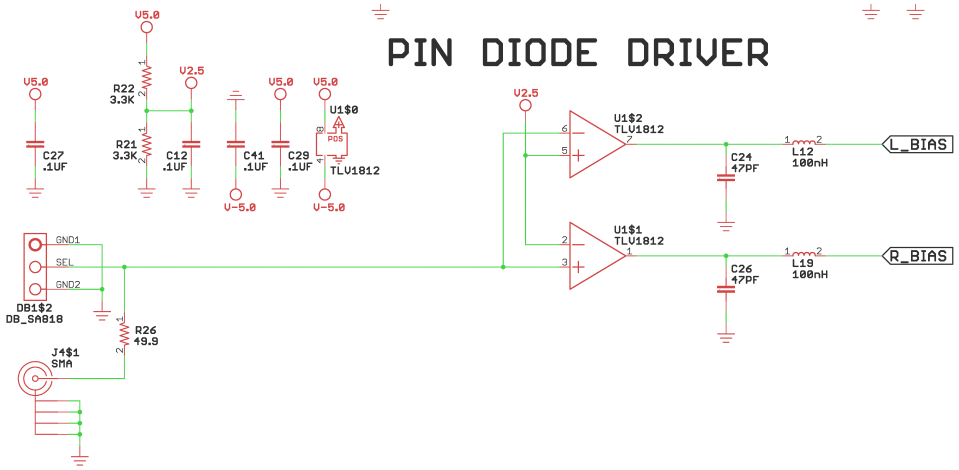


Figure 4.31: Next

The antenna switch driver matches the method used on the 102-73174-71 board. The 102-73174-71 board provides for forward bias from the +5V supply while reverse bias comes from the negative supply. This change reduces the current demand on the negative supply.

The driver (TLV1812) is a simple analog comparator that is powered from the +5V rail and then -5V rail. We then use a simple resistor divider to generate roughly 2.5V to compare the incoming clock against.

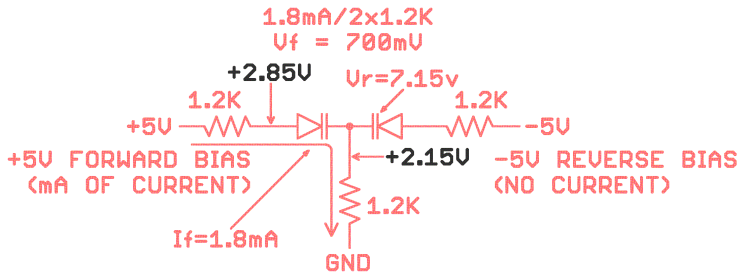


Figure 4.32: Biasing Model

The PIN diode biasing calculation model. (5.0V-0.7V)/2.4KΩ gives 1.79mA

The commmon cathode point is connected (through an RF choke and resistor) to ground. The two anodes are switched between the positive and negative supplies.

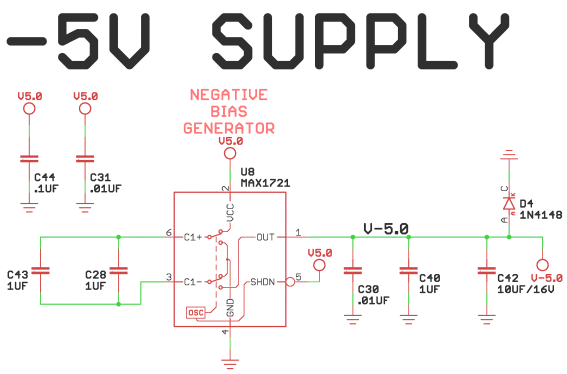
Assuming the current limiting resistors are the same value, the conducting diode will be sitting midway between the +5V rail and ground. Given a roughly 700mV drop, the diode anode and cathode of the forward biased diode will be at the indicated voltages.

The other diode in the pair will be reverse biased as the negative supply is gated on as shown. Since no current to speak of flows in the reverse direction, that diode will see a reverse voltage of just over 7 volts.

Although we could have a lower negative voltage (the 102-73174-82 board can produce lower negative rail) the -7V reverse bias puts the PIN diode into a very low capacitance high isolation region of operation.

The BAR63 series datasheet indicates a capacitance of about .2pF with a reverse bias of -5V. The datasheet indicates an RF impedance of near 500KΩ at the same -5V bias. The inseertion loss at -5V is shown as in excess of -20dB.

Driving around 2mA of forward current shows an RF impedance of about 2Ω.



313

Figure 4.33: Next

The -5V supply, a simple switched capacitor device that can supply over 10mA. This supply rail need only supply leakage current during steady state operation, well within the capability of a switched capacitor topology. The switching load will also be quite low as we are operating at audio frequencies, again well within the capability of this switched capacitor topology.

4.5 Dual Antenna Switch

Source File: FOX_zNEO_Theory_Operation_5.tex

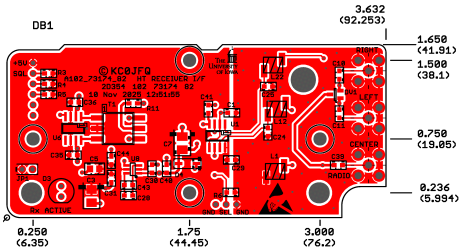


Figure 4.34: Dual Antenna Switch (102-73174-82)

This board provides a basic two antenna switch along the lines of the 102-73170-20 board but clocked by the zNEO on the main board.

There are two antenna element connectors, labeled ***RIGHT*** and ***LEFT***, and one radio connector labeled ***CENTER***.

PIN diode drive

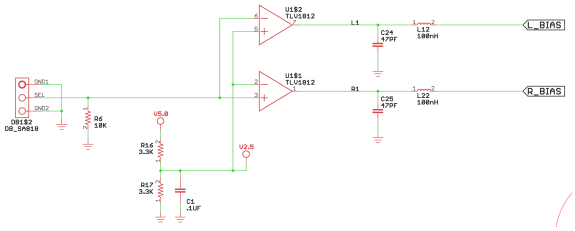


Figure 4.35: PIN Drive Schematic (102-73174-82)

Simple bipolar drive using an analog comparator powered from the +5V rail and the -5V rail.

This configuration has one diode forward biased and the other reverse biased. We receive a 50% duty cycle square wave on the **SEL** net coming in through the **DB1$2** connector.

PIN diode antenna switch

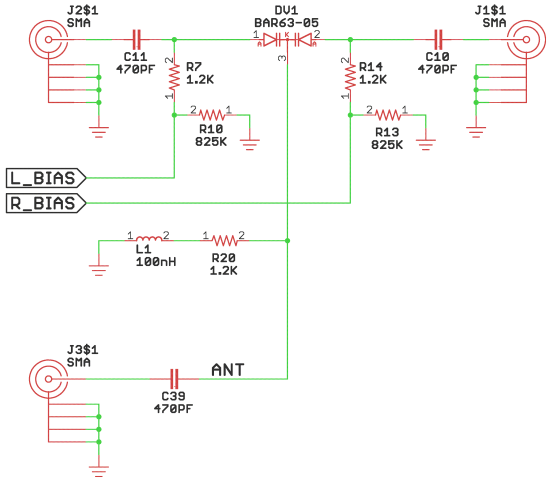


Figure 4.36: PIN Diode Schematic (102-73174-82)

Same PIN diode switch used everywhere. **L_BIAS** and **R_BIAS** are always the opposite polarity.

Negative Supply

Choose only one to populate!

Two variants appear on the board, one being able to produce a more negative value than the other. The schematic will be updated after some testing.

-5V supply

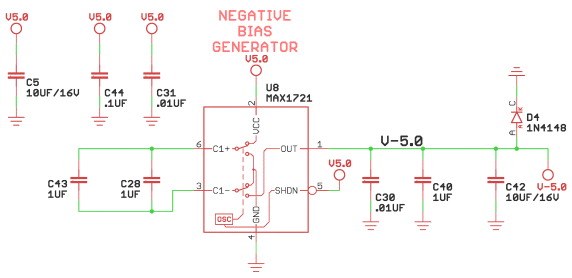
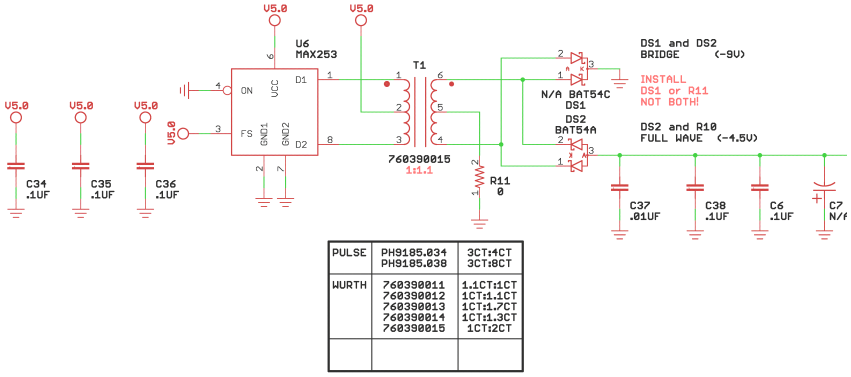


Figure 4.37: Switched Capacitor Convertor (102-73174-82)

Simple switched capacitor design taken from the MAX1721 datasheet.

The negative supply provides reverse bias for the PIN diode with no current demand. The switched capacitor design easily provides the current spikes that occur during switching of the PIN diode.

-9V supply



PULSE	PH9185.031 PH9185.038	3CT:1CT 3CT:8CT
WURTH	760390011 760390012 760390013 760390014 760390015	1.1CT:1CT 1CT:1.1CT 1CT:1.7CT 1CT:1.3CT 1CT:2CT

Figure 4.38: Transformer Convertor (102-73174-82)

Should a higher reverse voltage be required on the PIN diode, we can switch over to using a transformer design. Here we can simply choose an appropriate turns ratio to target the bias voltage. The topology also allow for re-confuguring the diode bridge.

4.6 Antenna Base

Source File: FOX_zNEO_Theory_Operation_6.tex

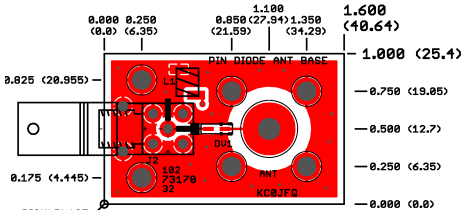


Figure 4.39: Antenna Base (102-73170-32)

The antenna base provides a convenient means of mounting an an ad-hoc antenna element. All the board provides for is a connection point for cables back to the antenna switching box.

The hole patterns will also allow for a flange mount BNC to be used if it is mounted on short spacers.

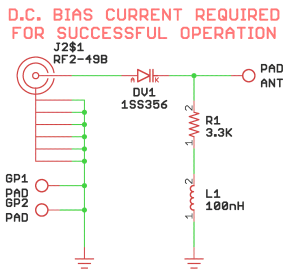


Figure 4.40: Antenna Base Schematic (102-73170-32)

The board also provides for mounting a PIN diode to improve isolation should the need arise. In most cases, the DV1 position is shorted and the resistor and inductor are left off.

The antenna cable, on the left, carries the DC bias to the PIN diode DV1. To bias the diode on, approximately 5 volts must be supplied. To bias the diode off, a negative voltage is delivered. In the case of the antenna rotator, about -9V is provided.

Chapter 5

Commanding

Source File: FOX_zNEO_Commanding.tex

Control and Configuratiopn commands.

These are take from the Fox Transmitter software.

5.1 Commands

Blah Blah Blah

5.1.1 FREQ

Source File: FOX_zNEO_Command_FREQ.tex

Table 5.1: Transmit carrier frequency control

Command sample	Description
FREQ *freq*	Operating Frequency

Action:

Select the Transmitter Operating Frequency.

This new frequency selection will be loaded into the RF subsystem.

Arguments:

Frequency, in MHz.

The action performed depends on the transmit element selected in the **CONF** command.

DRA818/SA818

Transceiver Module

The frequency string must be...

EXTERN

External Handie Talkie

The frequency string will need to be massaged into the appropriate setup commands for the handie-talkie in use. The V3.70 software does not handle any handie-talkie.

Frequency Limiting

The **FREQ** handler does very minimal limits checking to try to keep frequency selection sane. All operating frequencies have been migrated to external tables, so effect any required limits by loading tables with valid entries.

Chapter 6

[13]

Assembly Notes

Source File: FOX_zNEO_Assembly.tex

Construction Notes.

6.1 Main Board Notes

Source File: FOX_zNEO_Assembly.tex

This section concerns the 102-73174-51 board.

6.1.1 Compass Display Assembly

Nine LEDs form a meter or compass display. This is directly controlled by the zNEO using the PE and PG pins. Software determines if it acts as a compass display or as a meter display.

Overlaying the daughtercard in section 4.25 on page 25 on top of the main board you will notice overlap between LED-1, LED-2, LED-8 and LED-9. The other daughtercard from section 4.24 on page 25 is notched to clear all of the LEDs.

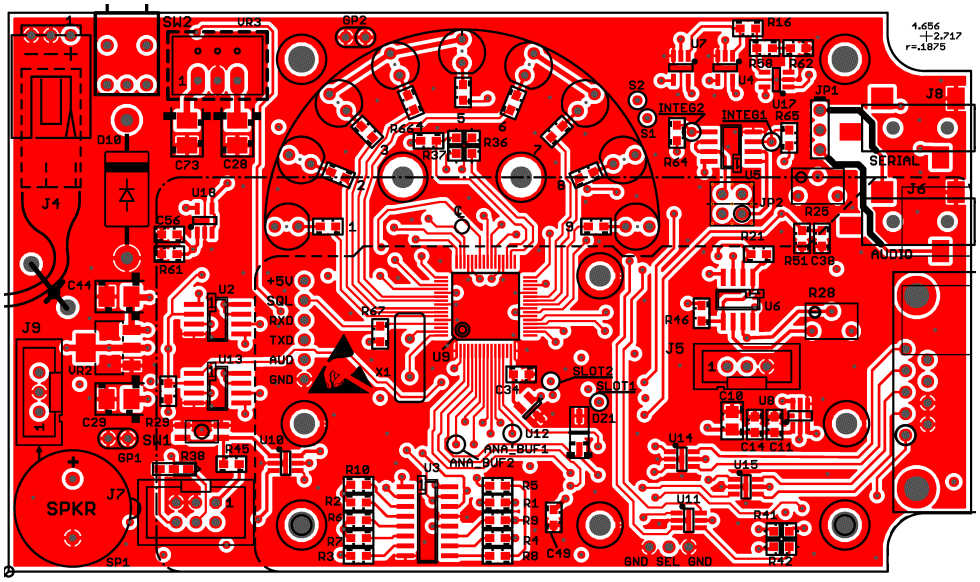


Figure 6.1: Daughter Card Overlap

The LEDs may be installed pointing down, away from the daughtercard, protruding through the bottom of the enclosure.

Also note that the meter LED array is a single library part. This locks the placement of the LEDs and resistors when the library part is built. This also allows the meter array to be placed on the board while keeping all parts correctly oriented.

This method does present a bit of a problem in that the LEDs and resistors are not individually called out in the parts list. Rather the meter array is a single part in the parts list.

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6.1.2 Main board J6 connector

The J6 connector is the audio in connector. It should be populated **only** when the board will be used with an external receiver.

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6.1.3 Main board J7 connector

The J7 connector is the zNEO programming header. When using the 102-73174-91 daughter card, this connector is obscured or blocked making re-programming the SOC potentially rather difficult.

For the purposes of software debugging, a *tall standing* daughter card may be fabricated with abnormally long interconnect pins and corresponding spacers. All the interconnect signals are low bandwidth so debugging with an extended daughter card should not present any functional issues.

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